

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E.

Branch: ES – Cluster Elective

Course Code: 19EC7CE2LV

Course: Low Power VLSI

Semester: VII

Duration: 3 hrs.

Max Marks: 100

Date: 28.02.2023

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

- 1 a) Explain the latch-up problem of CMOS devices. How can it be overcome? **10**
- b) Discuss the switching characteristics of a CMOS inverter and obtain an estimate of the inverter delay. **10**

UNIT - II

- 2 a) With the help of a neat circuit diagram, briefly explain the working of a domino CMOS logic circuit. **08**
- b) List the Various mechanisms which affect the sub threshold leakage current and explain any two in detail. **08**
- c) A 32 bit off-chip bus operating at 4.8 Volt and 64 MHz clock rate is driving a capacitance of 25 pF/bit. Each bit is estimated to have toggling probability of 0.25 at each clock cycle. What is the power dissipation operating the bus? **04**

UNIT - III

- 3 a) Distinguish between constant-field and constant-voltage feature size scaling **08**
- b) Explain Multilevel Voltage Scaling and discuss the challenges in its implementation. **12**

UNIT - IV

- 4 a) What are the different clock gating cells and explain them. **06**
- b) What are Glitches? What is the effect of Glitches on power consumption? How are they minimized? **06**
- c) Explain the concept of bus encoding, and explain the different types of encoding with a neat diagram. **08**

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

OR

- 5 a) Draw the circuit diagram of MTCMOS and VTCMOS inverter circuit. **10**
Analyze their leakage power optimizing principle.
- b) Illustrate the transistor stack effect. How can it be used to reduce leakage power dissipation in standby mode? **10**

UNIT - V

- 6 a) Discuss the basic principle of Adiabatic Amplification with neat diagram **10**
- b) Define the term energy density in battery, discuss on any 2 popular rechargeable battery technologies **10**

OR

- 7 a) Prove that the charging of a capacitor C in n steps to a voltage V_{DD} instead of a conventional single-step charging reduces the power dissipation by a factor of n . Discuss the disadvantages of this stepwise charging circuit. **10**
- b) Indicate the significance of a battery-aware task scheduling technique in battery driven systems. **10**
