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B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VII**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC7CE2SC **Max Marks: 100**
Course: System On Chip **Date: 12.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1. a) Compare the various existing hardware and software implementations. Comment on the performance and programmability for various architectures. **10**

   b) Suggest a suitable processor architecture to implement sequential instruction execution. What are the drawbacks of this architecture? **10**

OR

2. a) It is required to speed up the process of virtual memory addressing. Suggest an appropriate approach to achieve the same. **10**

   b) Describe the significance of SIMD architectures in detail. **10**

UNIT - II

3. a) Discuss the effect of interlocks in Decoder functions. **10**

   b) Describe the functioning of a generic vector processor emphasizing the importance of vector chaining. **10**

OR

4. a) Describe the process of selecting processors emphasizing on processor core. **10**

   b) Discuss the architecture and working of the datapaths in generic VLIW processor **10**

UNIT - III

5. a) Differentiate between spiral and waterfall models. Justify the significance of spiral model. **10**

	b)	Explain the system design process which employs both executable and written specifications.	**10**

UNIT - IV

6.	a)	Suggest suitable timing closure techniques at both block level and system level	**10**
	b)	Discuss the physical design issues for timing closure.	**10**

UNIT - V

7.	a)	Discuss the various specifications required to understand the suitable interconnect architecture.	**10**
	b)	Suggest a typical bus based system designed to implement a multimaster system and explain the same.	**10**

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