U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January 2024 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC7CE2SC **Max Marks: 100**
Course: System on Chip

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Suggest a suitable processor architecture that can be used to carry out the execution of instructions sequentially and discuss its pros and cons.	*CO3*	*PO3*	**10**
	b)		Provide a simplified technology comparison of programmability versus performance using an appropriate graphical representation. Discuss the advantages and disadvantages of hardware and software implementation.	*CO3*	*PO3*	**10**
			OR			
2	a)		With the help of supportive architecture analyze the importance of VLIW processors.	*CO3*	*PO3*	**10**
	b)		Categorize and analyze the various approaches used for SoC interconnects.	*CO3*	*PO3*	**10**
			UNIT - II			
3	a)		Summarize the procedure for choosing processors, with a focus on the processor core.	*CO 2*	*PO 2*	**10**
	b)		Classify the instruction sets for basic architecture.	*CO 2*	*PO 2*	**10**
			OR			
4	a)		Suggest two methods used to solve the branch problem? Discuss in detail.	*CO 2*	*PO 2*	**10**
	b)		Elucidate how a generic vector processor works, highlighting the significance of vector chaining.	*CO 2*	*PO 2*	**10**
			UNIT - III			
5	a)		Discuss the advantages and disadvantages of water fall and spiral design flow.	*CO 1*	*PO 1*	**10**
	b)		Highlight the significance of Hard IP and Soft IP in SoC.	*CO 1*	*PO 1*	**10**

			UNIT - IV			
	6	a)	Elucidate the significance of Interfaces to address the Logic design issues for timing closure.	***CO 3***	***PO 3***	**10**
		b)	Elaborate on the various ways that power dissipations occur in CMOS circuitry.	***CO 1***	***PO 1***	**10**
			UNIT - V			
	7	a)	Discuss various system level issues and specifications that need to be taken into consideration in order to select an appropriate interconnect architecture, using a supporting diagram of a SoC module in the context of the system.	***CO 3***	***PO 3***	**10**
		b)	Analyze the different possible bus designs with varying combinations of physical bus widths and arbitration protocols	***CO2***	***PO2***	**10**

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