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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC7CE2SC **Max Marks: 100**
Course: System On Chip **Date: 28.02.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Compare the various existing hardware and software implementations. Comment on the performance and programmability for various architectures.	**10**
	b)	"Exploiting program parallelism is one of the most important goals in computer architecture" Justify the statement considering the importance of classification of different computer processor architectures.	**05**
	c)	Briefly describe processors with memory off the chip on a multidie module.	**05**

OR

2	a)	Suggest a suitable mechanism to achieve Virtual - to - real address mapping and describe the implementation of the same.	**10**
	b)	Describe the architecture and instruction timing of a pipelined processor.	**10**

UNIT - II

3	a)	Describe with a suitable examples and flow diagram, the processor core selection.	**10**
	b)	With a neat diagram illustrate the overall layout of an M pipelined processor which inspects N instructions by issuing M instructions.	**06**
	c)	Classify the basic architectures of Common instruction sets.	**04**

OR

4	a)	Brief the significance of branch prediction. Classify and explain the same.	**10**
	b)	Discuss the architecture and working of the data paths in generic VLIW processor.	**10**

UNIT - III

5	a)	Describe the top level System Design Process flow for executable and written specifications.	**10**

b) "The traditional model for ASIC development in the project transitions from phase to phase in a step function, never returning to the activities of the previous phase." Identify the model which describes the feature specified and explain the same. **10**

UNIT - IV

6 a) Discuss the importance of Interfaces to address the Logic design issues for timing closure. **10**

b) "Most portable devices need low power designs"-Justify the statement highlighting the types of power dissipations in CMOS circuits. **10**

UNIT - V

7 a) "Unlike most bus architectures designed for PCB - based systems, the AMBA AHB bus avoids tristate implementation"- Propose the solution and describe in detail to address the problem in AMBA AHB. **10**

b) "NOC systems can be adapted more easily to the rapid advances in process technology or in system architecture."- Justify the statement. **10**

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