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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 22EC7PE3PD **Max Marks: 100**

Course: Physical Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	What is ESD event? Discuss the ESD protection circuits to prevent ESD event.	CO1	--	8
	b)	What are standard cells? Predict the average propagation delay of a standard inverter cell and estimate the channel dimension of the PMOS and NMOS so as to have optimum rise and fall time	CO1	--	12
		OR			
2	a)	Explain the physical design flow for an integrated circuit.	CO1	--	6
	b)	What is Electro-Static Discharge and how does it impact integrated circuits? With the help of neat diagrams, briefly discuss circuits to prevent such events.	CO1	--	8
	c)	Explain the following input files in physical design: (i) .db file (ii) .def file	CO1	--	6
		UNIT - II			
3	a)	Explain the constructive partitioning techniques.	CO1	--	10
	b)	Highlight the limitations of KL algorithm and describe any two extensions to overcome the same.	CO2	PO1	10
		OR			
4	a)	What is meant by Multilevel Partitioning? Demonstrate the use of clustering in accomplishing the same.	CO2	PO1	10
	b)	Explain Cluster growth and Hierarchical partitioning techniques.	CO1	--	10
		UNIT - III			
5	a)	Explain the rectangular dual graph technique with a suitable example. Also specify its drawbacks and methods to overcome the same.	CO1	--	10

		b)	For the given normalized polish expression `NPE = 25V1H374VH6V8VH`, obtain the slicing tree and apply the simulated annealing technique to obtain the optimized floorplan, given that the (width, height) of modules 1 through 8 are respectively {(2,4),(1,3),(3,3),(3,5),(3,2),(5,3),(1,2),(2,4)}. Compute the change in area.	***CO2***	***PO1***	**10**
			OR			
	6	a)	Discuss the simulated annealing technique for placements with an algorithm, perturb function and Timberwolf schedule function. Also explain the move restrictions with relevant equations.	***CO1***	--	**10**
		b)	Consider the force directed placement problem applied to a 4×4 grid. Assume that four blocks A, B, C and D are already pre-placed on the grid locations (0,3), (3,3), (0,0) and (3,1) respectively. A new block *S* is required to be placed where the weights with respect to the already placed blocks are: w_{SA} = 10, w_{SB} =4, w_{SC} =8 and w_{SD} =3. What will the zero-force target location of block *S* be? Place the blocks on a 4×4 grid.	***CO2***	***PO1***	**10**
			UNIT – IV			
	7	a)	Discuss the important of clock tree synthesis. What are the goals of clock routing algorithms?	***CO2***	***PO1***	**08**
		b)	Discuss the set-up time and hold time constraints in presence of skew with relevant diagrams and equations. Discuss the various clock tree routing problem formulations.	***CO1***	--	**12**
			OR			
	8	a)	Discuss the set-up time and hold time constraints with relevant diagrams and equations.	***CO1***	--	**10**
		b)	Apply the concept of clock skew to determine its effect on timing constraints of flip flop-based synchronous design. Briefly describe H-tree clock routing with the help of an example and highlight its advantages.	***CO2***	***PO1***	**10**
			UNIT - V			
	9	a)	Write a short note on (i) DRC (ii) ERC and (iii) LVS.	***CO1***	--	**10**
		b)	Briefly discuss (i) Channel routing (ii) Switchbox routing and (iii) *Over-the-cell* (OTC) routing.	***CO1***	--	**10**
			OR			
	10	a)	Discuss global routing in the contexts of Full-custom design, Standard-cell design and Gate-array design.	***CO1***	--	**10**
		b)	What is electromigration? Discuss the various methods to fix electromigration.	***CO1***	--	**10**

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