U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 16EC7DCESD **Max Marks: 100**
Course: Embedded System Design **Date: 20.02.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	With a neat diagram discuss the various components of embedded system hardware.		**10**
	b)	Discuss the various models in the Embedded Systems Architecture design.		**10**

UNIT - II

2	a)	Draw the Instruction Level Parallelism processor architecture and analyse the execution flow through each stage of its pipeline.		**10**
	b)	Given the following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations. (i) 4 Kbyte, 8-way set-associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles. (ii) 8 Kbyte, 4-way set-associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles. (iii) 16 Kbyte, 2-way set-associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles.		**10**

OR

3	a)	Design a 32X4 RAM module using 8X4 RAM chips - Assume an 8-address line processor.		**10**
	b)	What are the solutions for improving the bandwidth of main memory in an Embedded System.		**10**

UNIT - III

4	a)	List and define the six main logical units of the I/O hardware.		**08**
	b)	With a neat diagram, discuss the three bus arbitration schemes used for embedded buses		**12**

OR

5	a)	Discuss the logical components (engines) of I/O graphics on an embedded board with a neat diagram.		**10**

	b)	With a neat timing diagram, discuss the data transfer in I2C bus, highlighting the most significant features of I2C bus.	**10**

UNIT - IV

6	a)	Discuss Device drivers with neat illustrations.	**10**
	b)	Write the I2C device driver pseudocode.	**10**

UNIT - V

7	a)	What is Middleware? Discuss General Purpose and Market specific middleware.	**10**
	b)	What is an application software? Discuss in detail.	**10**

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