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B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7PCESD **Max Marks: 100**
Course: Embedded System Design **Date: 13.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1. a) Define embedded system. With a generic block diagram, explain how the embedded system works. **07**

   b) Define communication interface. If an input device has to send data to a computing unit through port B of 8255 PPI using handshake mode, draw the schematic and find out the control word for configuration. **08**

   c) Analyze the utility of a watch dog timer in an embedded system. **05**

UNIT - II

2. a) Differentiate between the polling and the interrupt methods of I/O operation. **04**

   b) Design the memory composition using 4KB of RAM to build 16KB of storage space required for an embedded system. Assume the initial address is 0XC000. Show the address range of each memory block. **08**

   c) What is a communication protocol? Compare the features of I2C and SPI protocols. **08**

OR

3. a) Identify the need of a cache memory? Given a direct mapped cache memory of size 2KB and the cacheline length is 32Bytes. If processor has to search the data from address 0XABCD, find out the offset, cacheline index and tag bits. Also how many blocks from the main memory are mapped to one block in cache memory? **08**

   b) Illustrate the workflow of Direct Memory Access Controller when an input device gives a DMA request. **08**

   c) Mention the features of USB protocol. **04**

UNIT - III

4. a) What is embedded firmware? Discuss the Superloop and RTOS approaches of firmware design. **10**

   b) Write an embedded C program to transfer a message "Hello world\n" at 9600 baud rate through UART0 of LPC 1768 controller. Assume the bit-7 of the LSR shows '1' when the transmit and holding register (THR) is empty to receive data from controller. Assume the peripheral clock as 4MHz and initialize LCR, DLM and DLL appropriately. **10**

OR

5. a) Write an embedded C program to display digits 1,2,3 and 4 in a sequence on a common cathode 7-sement display at GPIO port-0 of LPC 1768 controller. Assume the port pins for datalines and enable of the display as: **10**

   Port0- pin8- pin15 : D0-D7 respectively.

   Port0-pin7- display enable.

   b) Write a psuedocode for data communication between a master controller and an output slave device over I2C protocol. **10**

UNIT - IV

6. a) Three processes P1, P2, P3 with estimated completion time 8, 5, 3 ms respectively, enter the ready queue together in the order P3, P2, P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time in RR algorithm with Time slice=3ms **10**

   b) What is a semaphore? Consider two parallel processes P1 (producer) & P2 (consumer) share a common buffer. Write a pseudocode to implement semaphore protection for critical section. **10**

UNIT - V

7. a) Differentiate between native and cross compiler. Illustrate the flow of cross compilation. List out the files generated on cross compilation. **10**

   b) Mention the use of the following tools in embedded firmware development: **10**

   - IDE
   - Simulator
   - Emulator
   - Debugger

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