U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7PCESD **Max Marks: 100**
Course: Embedded System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Compare RISC V/s CISC Processor/Controllers.	CO2	PO2	6
	b)	What is the Significance of "Watchdog Timer" in Embedded Systems? For a watchdog timer working on 4 kHz clock and timeout time of 500ms, calculate the value of the counter.	CO1	PO1	7
	c)	Discuss the Operational and Non-operational quality attributes of embedded systems.	CO1	PO1	7
		OR			
2	a)	Compare General purpose system and Embedded system.	CO2	PO2	7
	b)	What is an embedded system? Discuss the role of sensors and actuators used in the embedded systems.	CO1	PO1	7
	c)	An integer variable with value 255 is stored in memory location at 0x8000. The processor word length is 8 bits and the processor is a big endian processor. The size of integer is considered as 4 bytes in the system. What is the value held by the memory location 0x8000.	CO1	PO1	6
		UNIT - II			
3	a)	Illustrate the functioning of I2C protocol when master device has to send data to a slave device on the bus. Draw the timing diagram. Compare with SPI communication protocol.	CO2	PO2	10
	b)	Illustrate the workflow of a DMA controller when an input device sends a DMA request. Why is DMA is preferred than interrupt for faster and bulk data transfer?	CO1	PO1	10
		OR			
4	a)	With a diagram, discuss the Set Associative mapping technique. Given a 2-level cache design where the hit rates are 88% for the smaller cache and 97% for the larger cache, the access costs for a	CO2	PO2	10

			miss are 12 cycles and 20 cycles, respectively, and the access cost for a hit is one cycle, calculate the average cost of access.			
		b)	Discuss arbitration in Priority and Daisy chain arbiters with neat illustrations	***CO1***	***PO1***	**10**
			UNIT - III			
	5	a)	Develop an embedded C code to interface a common cathode 7-segment display at GPIO port-0 of LPC 1768 controller.	***CO3***	***PO3***	**10**
		b)	Discuss the Super Loop approach with Pros, Cons and Enhancements.	***CO1***	***PO1***	**10**
			OR			
	6	a)	List the various Embedded firmware Development Languages/Options. With neat diagram, discuss the machine language conversion process.	***CO1***	***PO1***	**10**
		b)	Develop a device driver pseudocode for communication over I2C bus.	***CO3***	***PO3***	**10**
			UNIT - IV			
	7	a)	Compare non-preemptive Last come first serve and shortest job first scheduling. Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds and priorities 1, 3, 2 (0-highest priority, 3 lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6ms and priority 0 enters the 'Ready' queue after 5ms of start of execution of P1 in a preemptive priority based scheduling. Assume all the processes contain only CPU operation and no I/O operations are involved.	***CO1***	***PO1***	**10**
		b)	With neat diagram, discuss how memory mapped objects are used in Inter Process Communication.	***CO1***	***PO1***	**10**
			OR			
	8	a)	Using the dining philosophers problem, discuss the various synchronization issues.	***CO1***	***PO1***	**10**
		b)	What is Priority Inversion? Discuss the two techniques of Priority Inversion Avoidance.	***CO1***	***PO1***	**10**
			UNIT-V			
	9	a)	Discuss the various techniques available for embedded firmware debugging.	***CO1***	***PO1***	**10**
		b)	Justify the need for cross compilation. Compare and contrast compilation and Cross Compilation.	***CO2***	***PO2***	**10**
			OR			
	10	a)	With neat diagram, discuss the various components required for an Embedded System Development Environment	***CO1***	***PO1***	**10**
		b)	Discuss in detail the types of files generated during cross-compilation of an Embedded C Code	***CO1***	***PO1***	**10**

*****