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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7PCESD **Max Marks: 100**
Course: Embedded System Design **Date: 20.02.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Differentiate an Embedded System from a general purpose computing system. Illustrate how endianness affects the processor operation in a multibyte system when a 4 byte long integer is stored in a memory with the base address being 0x20000.	**10**
	b)	List the various non-operational quality attributes that need to be addressed for designing an embedded product. Illustrate the different stages of a product life cycle curve.	**06**
	c)	Compare and comment on the Von Neumann and Harvard architectures used in processor design.	**04**

UNIT - II

2	a)	With a flowchart, explain peripheral to memory transfer without DMA, using vectored interrupt. Peripheral receives input data in a register with address 0x8000 and interrupt address vector is 16.	**08**
	b)	Given a 2-level cache design where the hit rates are 88% for the smaller cache and 97% for the larger cache, the access costs for a miss are 12 cycles and 20 cycles, respectively, and the access cost for a hit is one cycle, calculate the average cost of access.	**06**
	c)	Suggest the most suitable onboard communication interface for applications requiring transfer of data in 'streams' and elaborate on the various features and working principle of the same.	**06**

OR

3	a)	Given design with cache implemented has a main memory access cost of 20 cycles on a miss and two cycles on a hit. The same design without the cache has a main memory access cost of 16 cycles. Calculate the minimum hit rate of the cache to make the cache implementation worthwhile.	**06**
	b)	Distinguish between using memory-mapped I/O and standard I/O.	**04**
	c)	With a neat I2C bus interfacing diagram, discuss the sequence of operation for communicating with an I2C slave device, highlighting the data rates of I2C bus.	**10**

UNIT - III

4	a)	Analyse the need for assembly language based development as a common technique for embedded technology**.** Illustrate the various steps involved in the conversion of program written in assembly language to corresponding machine language.	**10**
	b)	Write an embedded C program to interface a common cathode 7-sement display at GPIO port-0 of LPC 1768 controller. Assume the port pins for data lines and enable of the display.	**10**

OR

5	a)	Ilustrate with examples, the two basic approaches used for Embedded firmware design.	**10**
	b)	Write an embedded C program to interface a DC motor with ARM processor LPC 1768 using UART in order to control the direction of rotation.	**10**

UNIT - IV

6	a)	Three processes with process IDs P1, P2, P3 with estimated completion time 10,5,7 milliseconds respectively, enters the ready queue together in the order P1, P2, P3. If a new process P4 with estimated completion time of 2ms enters the ready queue after 2 ms of execution of P2, Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes) in SJF scheduling and SJF preemptive scheduling . Assume all the processes contain only CPU operations and no I/O operations are involved. Hence compare preemptive and non-preemptive SJF scheduling.	**10**
	b)	What is Priority Inversion? Explain any two methods to handle priority inversion problem**.**	**10**

UNIT - V

7	a)	Consider a scenario where the embedded C code needs to be converted to a target processor using ARM processor. Analyse the various file that will be generated during this process.	**10**
	b)	Differentiate between ‘simulator’ and ‘emulator. Discuss the various features of simulator based firmware debugging which make it so popular	**10**

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