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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2025 Semester End Make-Up Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 22EC7PCESD **Max Marks: 100**

Course: Embedded System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Describe the core components of an embedded system.	*CO 1*	-	**5**
	b)		Analyze the operation of a watchdog timer to ensure proper operation of an embedded system.	*CO3*	*PO2*	**5**
	c)		An embedded system design needs an 8KX8 RAM module. Design an 8KX8 RAM module using 2KX8 RAM chips. The module should be connected on an 8-bit processor with a 16-bit address bus, and occupy the address range starting from the address A000. Show the circuit and the memory map.	*CO 4*	*PO 3*	**10**
			OR			
2	a)		Discuss the various classifications of an embedded system. Give an example for each.	*CO 1*	-	**5**
	b)		Analyze the different quality attributes to be considered in an embedded system design.	*CO 3*	*PO 2*	**5**
	c)		For an embedded system design, i) Compose 1K x 8 ROMs into a 2K × 16 ROM. ii) Design an internal structure of an 8x4 ROM using a 3x8 decoder, Consider an input address of "010."	*CO 4*	*PO 3*	**10**
			UNIT - II			
3	a)		Justify the use of a barrel shifter with an ALU to improve the power and flexibility of many data processing operations. Consider an ARM assembly instruction: LSL R0, R1, #3 Show the Step-by-Step breakdown of the operation assuming R1 contains the number 5.	*CO 3*	*PO 2*	**10**
	b)		Illustrate with examples the classification of ARM instruction set.	*CO 1*	-	**5**

		c)	Indicate how the CPSR that resides in the register file of the ARM core is used to monitor and control internal operations.	*CO2*	*PO1*	**5**
			OR			
	4	a)	Analyze the programmer's model of the ARM Cortex-M3 processor and indicate how the different register sets, including general-purpose registers, special-purpose registers, and status registers influence the execution of code.	*CO 3*	*PO2*	**10**
		b)	Differentiate ARM and Thumb instruction set features.	*CO2*	*PO1*	**5**
		c)	Elaborate with the help of memory map, the memory features of Cortex M3.	*CO1*	-	**5**
			UNIT - III			
	5	a)	Differentiate between I2C and SPI communication interface.	*CO1*	-	**5**
		b)	Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find 1. Number of Bits in Physical Address 2. Number of Bits in Block Offset 3. Number of Bits in Tag 4. Number of Lines in Cache 5. Tag Directory Size .	*CO2*	*PO1*	**10**
		c)	What is bus arbitration? Explain the different bus arbitration schemes used for embedded system buses.	*CO1*	-	**5**
			OR			
	6	a)	Illustrate data transaction using I2C communication protocol. Draw the timing diagram. Mention its features.	*CO1*	-	**6**
		b)	Given the following three cache designs, analyse the one with the best performance by calculating the average cost of access. Show all calculations. (a) 4 Kbyte, 8-way set-associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles. (b) 8 Kbyte, 4-way set-associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles. (c) 16 Kbyte, 2-way set-associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles.	*CO2*	*PO1*	**10**
		c)	Discuss the advantages and disadvantages of using memory-mapped I/O versus standard I/O.	*CO1*	-	**4**
			UNIT - IV			
	7	a)	Analyse the different types of files generated by a cross-compiler during the build process, and discuss the role of each file in the compilation and execution of embedded applications.	*CO3*	*PO2*	**8**
		b)	Illustrate with examples, the two basic approaches used for Embedded firmware design.	*CO1*	-	**7**
		c)	Write an embedded C program to interface the 7 segment display with ARM processor LPC 1768 using UART.	*CO4*	*PO3*	**5**

			OR			
	8	a)	Analyse the various steps involved in the conversion of program written in assembly language to corresponding machine language.	*CO3*	*PO2*	**8**
		b)	Differentiate the function of 'simulator' and 'disassembler'. Discuss the various features of simulator-based firmware debugging which make it so popular, also mention any limitation in this type of debugging.	*CO1*	-	**7**
		c)	Write an embedded C program to interface a DC motor with ARM processor LPC 1768 in order to control the direction of rotation.	*CO4*	*PO3*	**5**
			UNIT - V			
	9	a)	The decision of an RTOS for an embedded design is very critical. Elaborate on the factors that need to be considered before making a decision on the selection of an RTOS.	*CO2*	*PO1*	**7**
		b)	Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds respectively enters the ready queue together in the order P1, P2, P3 (Assume only P1 is present in the 'Ready' queue when the scheduler picks up it and P2, P3 entered 'Ready' queue after that). Now a new process P4 with estimated completion time 6ms enters the 'Ready' queue after 5ms of scheduling P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes).Assume all the processes contain only CPU operation and no I/O operations are involved in Last In First Out (LIFO)scheduling algorithm.	*CO2*	*PO1*	**9**
		c)	Compare Binary Semaphore and Counting Semaphore.	*CO2*	*PO1*	**4**
			OR			
	10	a)	Compare a process and thread.	*CO2*	*PO1*	**4**
		b)	List the requirements of a good scheduling algorithm. How would you calculate the CPU utilization time if CPU time is 1 second of total execution time of 2 seconds?	*CO2*	*PO1*	**7**
		c)	Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds and priorities 1, 3, 2 (0-highest priority, 3 lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6ms and priority 0 enters the 'Ready' queue after 5ms of start of execution of P1. Assume all the processes contain only CPU operation and no I/O operations are involved. Determine the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time in Priority based Preemptive Scheduling.	*CO2*	*PO1*	**9**

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