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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 22EC7PCESD **Max Marks: 100**

Course: Embedded System Design

Instructions:1.Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define embedded system. With a generic block diagram, explain how the embedded system works.	CO 1	-	7
	b)	Analyze the utility of a watch dog timer in an embedded system.	CO 3	PO 2	5
	c)	Define communication interface. If an input device has to send data to a computing unit through port B of 8255 PPI using handshake mode, draw the schematic and find out the control word for configuration.	CO 2	PO 1	8
		OR			
2	a)	Analyse the various non-operational quality attributes that need to be addressed for designing an embedded product.	CO 3	PO 2	6
	b)	Briefly explain the utilities of sensors and actuators in embedded system design mentioning a few.	CO 2	PO 1	8
	c)	Classify embedded systems based on their computational capability.	CO 1	-	6
		UNIT - II			
3	a)	List the Special registers and its functions in Cortex M3 processors.	CO 1	-	5
	b)	List the advantages of Cortex M3 Processor. Compare ARM instructions with Thumb instructions.	CO 3	PO 2	10
	c)	Explain the programming status of control register that reflects the mode and use of MSP & PSP.	CO 1	-	5
		OR			
4	a)	Justify the use of a barrel shifter with an ALU to improve the power and flexibility of many data processing operations. Consider an ARM assembly instruction: LSL R1, R2, #2 Show the Step-by-Step breakdown of the operation assuming R1	CO 3	PO 2	10

			contains the number 4.			
		b)	Elaborate with the help of memory map, the memory features of Cortex M3. List the advantages of Cortex M3 processors.	***CO** 1*	-	**10**
			UNIT - III			
	5	a)	Differentiate between the polling, interrupt and DMA methods of I/O operation.	***CO** 3*	*PO 2*	**6**
		b)	With illustration, discuss the single master multi-slave communication over SPI protocol.	***CO** 1*	-	**10**
		c)	Mention the features of USB protocol.	***CO** 1*	-	**4**
			OR			
	6	a)	Analyze the workflow of Direct Memory Access Controller when an input device gives a DMA request.	***CO** 3*	*PO 2*	**10**
		b)	With a neat timing diagram, discuss the data transfer over I2C bus, highlighting the most significant features of I2C protocol.	***CO** 1*	-	**10**
			UNIT - IV			
	7	a)	Write an embedded C program to display “BMSCE” with ARM processor LPC 1768 using UART.	***CO** 4*	*PO 3*	**10**
		b)	With an example, discuss the Super-Loop and RTOS based firmware design approaches.	***CO** 1*	-	**10**
			OR			
	8	a)	Write an embedded C program to interface a Common Cathode 7-segment display with ARM processor LPC 1768.	***CO** 4*	*PO 3*	**10**
		b)	Discuss native and cross compilers. List out the files generated on cross compilation.	***CO** 1*	-	**10**
			UNIT - V			
	9	a)	Compare Preemptive and Non-preemptive based scheduling. Three processes P1, P2, P3 with estimated completion time 8, 5, 3ms respectively, enter the ready queue together in the order P3,P2, P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time in Round Robin algorithm with Time slice=3ms.	***CO** 2*	*PO 1*	**10**
		b)	What is a semaphore? Consider two parallel processes P1 (producer) & P2 (consumer) share a common buffer. Illustrate the use of Semaphore for this scenario.	***CO** 2*	*PO 1*	**10**
			OR			
	10	a)	Assume in a multiprocessing system, processes P1, P2 and P3 are having high, medium and low priority respectively. P1 and P3 share a common resource while P2 is independent. Apply a condition of priority inversion with an appropriate timing diagram. Justify how priority inheritance helps in reducing priority inversion.	***CO** 2*	*PO 1*	**10**
		b)	What is device driver? Mention its applications.	***CO** 2*	*PO1*	**10**

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