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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 22EC7PCESD **Max Marks: 100**

Course: Embedded System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)	Compare (i) Big Endian and Little Endian formats (ii) RISC vs CISC Processors		CO 3	PO 2	8
	b)	Design 32X4 RAM module using 8X4 RAM chips. Assume the processor is having 7 address line		CO 4	PO3	10
	c)	Justify the need for Commercial off the Shelf Component (COTS).		CO3	PO2	2
		OR				
2	a)	Discuss the Operational and Non-operational quality attributes of embedded systems. Analyze the Quality attribute that describes the new firmware or hardware technology.		CO3	PO2	10
	b)	For an embedded system design, i) Compose 1K x 8 ROMs into a 2K × 16 ROM . ii) Design an internal structure of an 8x4 ROM using a 3x8 decoder, Consider an input address of "010."		CO 4	PO3	10
		UNIT - II				
3	a)	With a neat block diagram, discuss the various components of cortex-M3 Architecture and the need for memory protection unit.		CO 1	-	10
	b)	Compare and show how ARM instruction set differs from the pure RISC.		CO3	PO2	5
	c)	List the advantages of Cortex M3 processors.		CO 2	PO1	5

			OR			
	4	a)	With a neat block diagram, discuss the functions of various components of LPC1768.	***CO 1***	-	**10**
		b)	Compare Thumb-2 instruction set and the Thumb instruction set.	***CO3***	***PO2***	**5**
		c)	List the special registers and it function in the Cortex-M3.	***CO 2***	***PO1***	**5**
			UNIT - III			
	5	a)	Using a flowchart, describe the process of peripheral-to-memory data transfer without DMA, triggered by a vectored interrupt when the peripheral receives input data in a register at address 0x8000, and the interrupt vector address is 16.	***CO 1***	-	**10**
		b)	Compare SPI with I2C protocol. Illustrate the functioning of SPI protocol when master device has to send data to a slave device on the bus. Draw the timing diagram.	***CO3***	***PO2***	**10**
			OR			
	6	a)	Compare the three common cache replacement policies. Given a 2-level cache design where the hit rates are 88% for the smaller cache and 97% for the larger cache, the access costs for a miss are 12 cycles and 20 cycles, respectively, and the access cost for a hit is one cycle, calculate the average cost of access.	***CO3***	***PO2***	**10**
		b)	Show the sequence of communication in a 1-Wire slave device with a neat diagram. List the main features of the 1-wire Interface.	***CO 1***	-	**10**
			UNIT - IV			
	7	a)	List the various Embedded Firmware Development Languages/Options. With neat diagram, discuss the machine language conversion process from high level language.	***CO 1***	-	**10**
		b)	Develop an embedded C program to interface a common cathode 7-sement display at GPIO port-0 of LPC 1768 controller.	***CO 4***	***PO3***	**10**
			OR			
	8	a)	Develop an embedded C program to interface a switch to interrupt the LPC 1768 controller externally and indicate the same on an LED.	***CO 4***	***PO3***	**10**
		b)	Discuss the types of debugging and highlight the features of simulator-based debugging.	***CO 1***	-	**10**
			UNIT - V			
	9	a)	Compare preemptive and non-preemptive Priority based scheduling. Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds and priorities 1, 3, 2 (0-	***CO 2***	***PO1***	**10**

			highest priority, 3 lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6ms and priority 0 enters the 'Ready' queue after 5ms of start of execution of P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time in a preemptive priority based scheduling. Assume all the processes contain only CPU operation and no I/O operations are involved.			
		b)	With a neat diagram, discuss the process states and their transitions. Discuss threads and processes.	***CO 1***	-	**10**
			OR			
	10	a)	What is priority Inversion? Discuss a suitable technique that can be used to avoid the same.	***CO 2***	***PO1***	**10**
		b)	With an example, discuss how counting semaphore and binary semaphore techniques are used for task synchronization.	***CO1***	-	**10**

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