U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May / June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VIII**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 22EC8PE4LV **Max Marks: 100**

Course: Low Power VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Elucidate the different types of process variations in semiconductor manufacturing and discuss their impact on circuit performance.	*1*	*1*	**10**
	b)		Analyze the latchup mechanism in CMOS circuits and its impact on circuit reliability. Justify how this latch up can be prevented.	*2*	*2*	**10**
			OR			
2	a)		Discuss on variation impacts which affect transistor ON and OFF currents and their influence on delay and energy. Analyze how yield is modeled using defect density.	*2*	*2*	**10**
	b)		Discuss why self-heating is still a major reliability risk in bidirectional wires, despite their lower susceptibility to electromigration compared to unidirectional wires.	*1*	*1*	**10**
			UNIT - II			
3	a)		Derive the expression for sub-threshold leakage current in MOS transistors and discuss its exponential dependence on the threshold voltage. Additionally, derive the sub-threshold slope (Ss) and discuss its significance in low-power circuit design.	*2*	*2*	**10**
	b)		Discuss the main energy-saving benefits of employing Dynamic Voltage and Frequency Scaling (DVFS) as opposed to merely frequency scaling, and how does the square-law relationship between power and voltage play a role in this?	*1*	*1*	**10**
			OR			
4	a)		Derive an expression for short-circuit power. How does the short circuit power vary with load capacitance?	*2*	*2*	**10**
	b)		What are the trade-offs between fine-grained and coarse-grained power gating in terms of area overhead and leakage power reduction?	*1*	*1*	**10**

			UNIT - III			
	5	a)	Design a circuit to compute F=AB+CD using NANDs and NORs. Also use bubble pushing to convert ANDs and ORs to three NANDs	*3*	*3*	**10**
		b)	Estimate the logical effort and parasitic delay of complex AOI Y=$\overline{(A.(B+C)+D.E)}$	*2*	*2*	**10**
			OR			
	6	a)	Design 3-input XOR functions using each of the following circuit techniques: a) Static CMOS b) Pseudo-nMOS c) Dual-rail domino	*3*	*3*	**10**
		b)	Sketch dynamic footed and unfooted 3-input NAND and NOR gates. Label the transistor widths. What is the logical effort of each gate?	*2*	*2*	**10**
			UNIT - IV			
	7	a)	Analyze power and delay for an inverter chain.	*2*	*2*	**10**
		b)	Briefly discuss different power saving techniques through gate reorganization and signal gating	*1*	*1*	**10**
			OR			
	8	a)	Discuss the basic architecture and signaling scheme of low swing bus.	*1*	*1*	**10**
		b)	Discuss power reduction techniques for a clock signal based on voltage swing reduction	*2*	*2*	**10**
			UNIT - V			
	9	a)	Analyze different trade-off approaches for task scheduling with voltage scaling.	*2*	*2*	**10**
		b)	What are the advantages and drawbacks of function in-lining in low-power system design?	*1*	*1*	**10**
			OR			
	10	a)	How does adiabatic logic differ from conventional CMOS circuits in terms of energy dissipation, and what are its practical limitations?	*1*	*3*	**10**
		b)	Analyze how dead-code elimination improves performance and reduce code size with examples.	*2*	*2*	**10**

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