U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June / July 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics & Instrumentation Engineering **Duration: 3 hrs.**
Course Code: 23EI5PCVLI **Max Marks: 100**
Course: VLSI DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		MODULE - I	CO	PO	Marks
1	a)	State and explain Moore's Law with relevant sketch.	CO1	-	**06**
	b)	Discuss fabrication process of an P-well process with neat diagram.	CO1	-	**10**
	c)	Compare Bipolar and CMOS Technologies	CO1	-	**04**
		OR			
2	a)	Derive pull up to pull down ratio of an NMOS inverter driven through one or More pass transistor	CO2	PO1	**10**
	b)	List out and discuss alternative forms of pull-up transistor	CO2	PO1	**06**
	c)	Discuss CMOS inverter with neat sketch	CO2	PO1	**04**
		MODULE- II			
3	a)	Obtain the scaling factor for the following parameter of a transistor a)Gate capacitance Cx b)Parasitic Capacitance Cx c)Saturation current I_{dss}	CO2	PO1	**06**
	b)	Construct schematic and CMOS stick Diagram for Y=$\overline{A + BCD}$	CO2	PO1	**06**
	c)	With neat sketches, Discuss the lambda based design rules for wires, NMOS,PMOS and CMOS transistor	CO2	PO1	**08**
		OR			
4	a)	Design briefly lambda based design rules for wires	CO3	PO3	**07**
	b)	What is the important of scaling? Find the scaling factors for Area, gate delay, power dissipation per gate, operating frequency	CO2	PO2	**07**
	c)	Design 1- bit shift register with neat sketch	CO3	PO2	**06**

			MODULE - III			
	5	a)	Design and implement Bus arbitration logic Using structured design along with stick diagram	*CO3*	*PO3*	**10**
		b)	What is parity generator and summarize briefly about structured design approach for the implementation of parity generator and also draw mos stick diagram for parity generator	*CO4*	*PO2*	**10**
			OR			
	6	a)	Discuss with neat sketch n-p CMOS and Dynamic CMOS three input Nand gate logic	*CO2*	*PO2*	**10**
		b)	Draw the schematic, stick diagram for nmos,CMOS and BICMOS 2 input Nand gate	*CO2*	*PO2*	**10**
			MODULE - IV			
	7	a)	Design four bit dynamic CMOS shift register using CMOS transmission gate switched logic and also draw the CMOS shift register cell.	*CO3*	*PO3*	**10**
		b)	With neat sketch Design and discuss 4X4 barrel shifter circuit.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Develop basic bus architectures design approach for the implementation of tentative floor plan for 4-bit data path.	*CO4*	*PO2*	**10**
		b)	Design Two-phase clock generator circuit using D flip flop	*CO3*	*PO3*	**10**
			MODULE- V			
	9	a)	Realize Three –transistor dynamic memory cell and also draw CMOS stick diagram.	*CO5*	*PO4*	**10**
		b)	Implement and discuss 4 T and 6 T dynamic and static memory cell.	*CO5*	*PO4*	**10**
			OR			
	10	a)	Implement and discuss nMOS and CMOS pseudo static Memory cell	*CO5*	*PO4*	**12**
		b)	Explain the optimization that can be applied for an CMOS inverter design	*CO5*	*PO4*	**08**

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