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# B.M.S.College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## January / February 2025 Semester End Main Examinations

**Programme: B.E.** **Semester: V**
**Branch: Electronics and Instrumentation Engineering** **Duration: 3 hrs.**
**Course Code: 23EI5PCVLI** **Max Marks: 100**
**Course: Basics of VLSI Design**

**Instructions**: 1.Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | | **MODULE - I** | *CO* | *PO* | **Marks** |
|---|---|---|---|---|---|---|
| 1 | a) | | With a neat diagram, discuss the importance of Moore's Law. With neat sketch and Explain Generations of an IC? | *CO1* | *PO1* | **06** |
| | b) | | Elaborate the various fabrication steps involved in fabrication of nMOS transistor | *CO1* | *PO1* | **10** |
| | c) | | Bring out the comparison between Bioplar and CMOS technologies | *CO1* | *PO1* | **04** |
| | | | **OR** | | | |
| 2 | a) | | Enlist the advantages and disadvantages of using Bi-CMOS technology in IC fabrication | *CO1* | *PO2* | **04** |
| | b) | | With relevant mathematical expression, derive pull up to pull down ratio of an NMOS inverter driven through one or More pass transistor. | *CO2* | *PO2* | **10** |
| | c) | | Highlight the process of Latch-Up in VLSI. List out and discuss the remedies that are to be considered to overcome the same. | *CO2* | *PO1* | **06** |
| | | | **MODULE - II** | | | |
| 3 | a) | | Discuss transistor design rules for NMOS, PMOS and CMOS transistor | *CO2* | *PO1* | **08** |
| | b) | | Suggest the alternative forms of pull up for an inverter configuration | *CO2* | *PO2* | **06** |
| | c) | | Obtain the scaling factor for the following parameter of a transistor<br>i) Power-speed Product $P_t$<br>ii) Maximum Operating Frequency $F_O$<br>iii) Saturation Current $I_{dss}$ | *CO2* | *PO2* | **06** |
| | | | **OR** | | | |
| 4 | a) | | With relevant diagram, discuss the working 1 bit shift register | *CO2* | *PO2* | **08** |

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| | | | showcasing different stages. | | | |
| | | b) | Draw the stick diagram for 2-input nMOS, 2-input NOR and 2-input NAND Gate | *CO2* | *PO2* | **08** |
| | | c) | Obtain the scaling factor for the following parameter of a transistor<br>i) Channel resistance $R_{ON}$<br>ii) Gate delay. | *CO2* | *PO3* | **04** |
| | | | **MODULE - III** | | | |
| | 5 | a) | Develop a structured design of a bus arbitration logic for a n line bus | *CO3* | *PO4* | **10** |
| | | b) | Discuss with neat sketch and relevant waveform Dynamic CMOS and Pseudo -nMOS logic | *CO3* | *PO4* | **10** |
| | | | **OR** | | | |
| | 6 | a) | Design, implement and explain NOR and Inverter gate using Clocked CMOS logic | *CO3* | *PO3* | **10** |
| | | b) | Explain structured design approach for the implementing parity generator. Draw nMOS stick diagram for parity generator | *CO3* | *PO4* | **10** |
| | | | **MODULE - IV** | | | |
| | 7 | a) | Implement and explain 4x4 barrel shifter. | *CO3* | *PO3* | **06** |
| | | b) | Discuss General Arrangement of a 4-bft Arithmetic Processor | *CO3* | *PO3* | **04** |
| | | c) | Describe the cascading structure of 4-bit nMOS dynamic shift register along with stick Diagram. | *CO3* | *PO3* | **10** |
| | | | **OR** | | | |
| | 8 | a) | Develop basic bus architectures design approach for the implementation of tentative floor plan for 4-bit data path | *CO3* | *PO2* | **10** |
| | | b) | Design and explain Two-phase clock generator circuit using D flip flop | *CO3* | *PO2* | **10** |
| | | | **MODULE - V** | | | |
| | 9 | a) | Discuss with neat sketch, Design Rule Checker and circuit extractor. | *CO4* | *PO12* | **10** |
| | | b) | With circuit diagram describe four transistor dynamic and six transistor Static CMOS memory cell. | *CO4* | *PO12* | **10** |
| | | | **OR** | | | |
| | 10 | a) | With neat sketch Discuss nMOS and CMOS Pseudo static memory cell | *CO5* | *PO12* | **10** |
| | | b) | Bring out a summative assessment of 3T dynamic RAM cell in terms of working, area occupied, dissipation and volatility. | *CO5* | *PO12* | **10** |



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