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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## September / October 2023 Supplementary Examinations

**Programme: B.E.** **Semester: VII**
**Branch: Electronics and Instrumentation Engineering** **Duration: 3 hrs.**
**Course Code: 19EI7PCVID** **Max Marks: 100**
**Course: VLSI Design** **Date: 12.09.2023**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.





### UNIT - I

| | | | |
|---|---|---|---|
| 1 | a) | State Moore's Law with neat sketch and explain generations of an IC? | **06** |
| | b) | Compare Bipolar and CMOS Technologies. | **04** |
| | c) | Discuss Twintub fabrication process with neat diagram | **10** |

**OR**

| | | | |
|---|---|---|---|
| 2 | a) | Mention the advantages and disadvantages of Bi-CMOS invertor. | **04** |
| | b) | Derive pull up to pull down ratio of an NMOS inverter driven through one or more pass transistor. | **10** |
| | c) | Explain latch-up problem in CMOS circuit and list the remedies to overcome it. | **06** |

### UNIT - II

| | | | |
|---|---|---|---|
| 3 | a) | Illustrate with neat sketches, explain the lambda based design rules for wires, NMOS and CMOS transistor. | **08** |
| | b) | Sketch the circuit, stick diagram and layout for a two input CMOS NOR gate. | **08** |
| | c) | Obtain the scaling factor for the following parameter of a transistor<br>1) Channel resistance Ron<br>2) Maximum Operating Frequency fo | **04** |

### UNIT - III

| | | | |
|---|---|---|---|
| 4 | a) | Develop a structured design of a bus arbitration logic for a n line bus | **07** |
| | b) | Draw circuit, CMOS stick diagram and layout for the equation Y= $\overline{(A.B)+(C.D)}$ | **07** |
| | c) | What is parity generator? explain structured design approach for the implementation of parity generator and also draw NMOS stick diagram for parity generator | **06** |

## UNIT - IV

| | | | |
|---|---|---|---|
| 5 | a) | Implement and explain 4x4 barrel shifter along with stick diagram | **06** |
| | b) | Discuss general arrangement of a 4-bit Arithmetic Processor | **04** |
| | c) | Describe the cascading structure of four-bit CMOS dynamic shift register along with stick diagram. | **10** |

## UNIT - V

| | | | |
|---|---|---|---|
| 6 | a) | Describe the CAD tools used for design and simulation of a chip | **10** |
| | b) | Sketch the circuit and working of three transistor dynamic RAM cell and also draw the stick diagram. | **10** |

**OR**

| | | | |
|---|---|---|---|
| 7 | a) | Derive and discuss optimization of NMOS and CMOS inverter | **10** |
| | b) | Sketch the circuit,stick diagram for an NMOS and CMOS pseudo static memory cell. Also, explain its working | **10** |

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