U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January 2024 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Instrumentation Engineering **Duration: 3 hrs.**
Course Code: 19EI7PCVID **Max Marks: 100**
Course: VLSI DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	State Moore's Law with neat sketch and Explain Generations of an IC?	CO1	-	**06**
	b)	Discuss NMOS fabrication process with neat sketch	CO1	-	**10**
	c)	Compare Bipolar and CMOS Technologies	CO1	-	**04**
		OR			
2	a)	Derive pull up to pull down ratio of an NMOS inverter driven through one or More pass transistor	CO2	PO1	**10**
	b)	List out and discuss alternative forms of pull-up transistor	CO2	PO1	**06**
	c)	Discuss NMOS inverter with neat sketch	CO1	-	**04**
		UNIT - II			
3	a)	Obtain the scaling factor for the following parameter of a transistor a)Gate capacitance Cx b)Parasitic Capacitance Cx c)Saturation current I_{dss}	CO2	PO1	**06**
	b)	Construct two input nmos NAND and NOR gate stick Diagram.	CO2	PO1	**06**
	c)	With neat sketches, Discuss the lambda based design rules for wires, NMOS and CMOS transistor	CO2	PO1	**08**
		UNIT - III			
4	a)	Design and implement Bus arbitration logic Using structured design along with stick diagram	CO3	PO3	**08**

		b)	What is parity generator and summarize briefly about structured design approach for the implementation of parity generator and also draw NMOS stick diagram for parity generator	*CO3*	*PO3*	**08**
		c)	Draw the General logic function block using two variable Technique.	*CO2*	*PO1*	**04**
			UNIT - IV			
	5	a)	Design four bit dynamic CMOS shift register using CMOS transmission gate switched logic and also draw the CMOS shift register cell.	*CO4*	*PO3*	**10**
		b)	Design and implement 4X4 barrel shifter circuit using 4x4 cross bar switch logic.	*CO4*	*PO3*	**10**
			UNIT - V			
	6	a)	Bring out a summative assessment of three transistor dynamic RAM cell in terms of Working, area occupied, dissipation and volatility	*CO5*	*PO3*	**10**
		b)	Implement and discuss optimization of CMOS inverter	*CO5*	*PO3*	**10**
			OR			
	7	a)	Implement and discuss NMOS and CMOS pseudo static Memory cell	*CO5*	*PO4*	**10**
		b)	Discuss the CAD tools used for design and simulation of a chip	*CO5*	*PO4*	**10**

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