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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Instrumentation Engineering **Duration: 3 hrs.**
Course Code: 19EI7PCVID **Max Marks: 100**
Course: VLSI Design **Date: 20.02.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Compare the Bipolar and CMOS Technologies. **04**

b) State Moore's Law. Explain Generations of an IC with a neat sketch. **06**

c) Describe the fabrication process of an NMOS transistor with a neat diagram **10**

OR

2 a) List the advantages and disadvantages of Bi-CMOS technology. **04**

b) Explain latch-up problem in CMOS circuit. List the remedies available to overcome latch-up problem. **06**

c) Derive the expression for a pull up to pull down ratio of an NMOS inverter driven through one or more pass transistor. **10**

UNIT - II

3 a) Suggest the alternative forms of pull up for an inverter configuration. **06**

b) Discuss the Lambda based design rules with respect to the followings: **08**

i. Wires
ii. NMOS transistor
iii. CMOS transistor.

c) Determine the scaling factor for the following parameter of a transistor **06**

i. Power-speed Product P_t
ii. Maximum Operating Frequency f_O
iii. Saturation current I_{dss}.

UNIT - III

4 a) What is parity generator? Explain structured design approach for the implementation of a parity generator and also draw NMOS stick diagram for the parity generator **06**

b) Develop a structured design of a bus arbitration logic for an n-line bus. **07**

c) Develop a CMOS stick diagram and layout for the expression $Y = \overline{(W.X) + (Y.Z)}$ **07**

UNIT - IV

5 a) Explain general arrangement of a 4-bit arithmetic processor. **04**

b) Implement and explain 4x4 barrel shifter along with stick diagram **06**

c) Discuss the cascading structure of 4-bit NMOS dynamic shift register along with a stick diagram. **10**

UNIT - V

6 a) Describe four transistor dynamic and six transistor static CMOS memory cell with circuit diagram. **10**

b) Describe the CAD tool used for design and simulation of a chip **10**

OR

7 a) Bring out a summative assessment of three transistor dynamic RAM cell in terms of working, area occupied, dissipation and volatility. **10**

b) Explain the optimization techniques with respect to area, switching power dissipation, asymmetry in rise and fall times and noise margin for a CMOS inverter. **10**

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