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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics and Instrumentation Engineering **Duration: 3 hrs.**

Course Code: 22EI7PCVLI **Max Marks: 100**

Course: VLSI Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

REAPPEAR EXAMS 2024-25

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			MODULE - I	*CO*	*PO*	Marks
1	a)		Compare the Bipolar and CMOS Technologies.	*CO1*	*PO1*	**05**
	b)		State Moore's Law. Explain Generations of an IC with a neat sketch.	*CO1*	*PO1*	**05**
	c)		Describe the fabrication process of an NMOS transistor with a neat diagram	*CO1*	*PO1*	**10**
			OR			
2	a)		List the advantages and disadvantages of Bi-CMOS technology.	*CO1*	*PO1*	**05**
	b)		Explain latch-up problem in CMOS circuit. List the remedies available to overcome latch-up problem.	*CO1*	*PO1*	**05**
	c)		Derive the expression for a pull up to pull down ratio of an NMOS inverter driven through one or more pass transistor.	*CO*	*PO2*	**10**
			MODULE- II			
3	a)		Suggest the alternative forms of pull up for an inverter configuration.	*CO2*	*PO2*	**10**
	b)		Discuss the Lambda based design rules with respect to the followings: i. Wires ii. NMOS	*CO2*	*PO2*	**05**
	c)		Determine the scaling factor for the following parameter of a transistor i. Power-speed Product Pt ii. Maximum Operating Frequency $f0$	*CO2*	*PO2*	**05**
			OR			
4	a)		What is the importance of Scaling? Find the scaling factors for Area, gate delay, Operating frequency and Power Dissipation	*CO2*	*PO2*	**10**

		b)	Design a CMOS logic circuit for the following function using minimum number of transistors and hence draw the stick diagram and layout. $Y = \overline{AB + CD}$	*CO3*	*PO3*	**10**
			MODULE - III			
	5	a)	What is parity generator? Explain structured design approach for the implementation of a parity generator and also draw NMOS stick diagram for the parity generator.	*CO3*	*PO3*	**10**
		b)	Develop a structured design of a bus arbitration logic for an n-line bus.	*CO3*	*PO3*	**10**
			OR			
	6	a)	Design 2 input NAND, NOR gates using **pseudo nMOS**, Dynamic CMOS	*CO3*	*PO3*	**10**
		b)	Develop a structured design of a bus arbitration logic for an Multiplexer.	*CO3*	*PO3*	**10**
			MODULE- IV			
	7	a)	Explain general arrangement of a 4-bit arithmetic processor.	*CO4*	*PO1*	**04**
		b)	Implement and explain 4x4 barrel shifter along with stick diagram	*CO4*	*PO3*	**08**
		c)	Discuss the cascading structure of 4-bit NMOS dynamic shift register along with a stick diagram	*CO4*	*PO2*	**08**
			OR			
	8	a)	Explain the general considerations in subsystem design processes for MOS circuits and also illustrate the design Process	*CO4*	*PO2*	**10**
		b)	Design a 4- Four-line Gray Code to Binary Code converter	*CO4*	*PO3*	**10**
			MODULE - V			
	9	a)	Explain the working principle of a one-transistor (1T) dynamic RAM cell. Discuss the role of the storage capacitor and access transistor in data storage and retrieval, along with the challenges of refresh cycles and data retention.	*CO5*	*PO1*	**10**
		b)	Describe the Computer-Aided Design (CAD) tools commonly used for the design and simulation of integrated circuits (chips).	*CO5*	*PO2*	**10**
			OR			
	10	a)	Evaluate the three-transistor (3T) DRAM cell in terms of working principle, area efficiency, power dissipation, volatility, and suitability for modern applications.	*CO5*	*PO2*	**10**
		b)	Explain nMOS pseudo static memory cell	*CO5*	*PO2*	**10**

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