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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## January / February 2025 Semester End Main Examinations

**Programme: B.E.** **Semester: VII**

**Branch: Electronics and Instrumentation Engineering** **Duration: 3 hrs.**

**Course Code: 22EI7PCVLI** **Max Marks: 100**

**Course: VLSI Design**

**Instructions**: 1. Answer an FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | | CO | PO | Marks |
|---|---|---|---|---|---|
| | | **MODULE - I** | | | |
| 1 | a) | Illustrate the fabrication of nMOS transistor with suitable diagram in detail. | *CO1* | *PO1* | **10** |
| | b) | Obtain the DC transfer characteristics of a CMOS inverter and mark all the region showing the status of PMOS and NMOS transistors. | *CO1* | *PO1* | **10** |
| | | **OR** | | | |
| 2 | a) | Discuss the action of enhancement mode transistor for different values of Vgs and Vds. | *CO1* | *PO1* | **10** |
| | b) | Describe in detail CMOS fabrication in an P-well process. | *CO1* | *PO1* | **10** |
| | | **MODULE - II** | | | |
| 3 | a) | Indicate the scaling factor for the following:<br>a) Gate capacitance<br>b) Maximum operating frequency<br>c) Current density<br>d) Power speed product | *CO2* | *PO2* | **10** |
| | b) | Draw the circuit and layout for inverter in CMOS style. | *CO2* | *PO2* | **10** |
| | | **OR** | | | |
| 4 | a) | Draw the circuit schematic and stick diagram of CMOS 2 input NAND gate. | *CO2* | *PO2* | **10** |
| | b) | Provide the $\lambda$-based design rules for transistors, contact cuts and vias. | *CO2* | *PO2* | **10** |
| | | **MODULE - III** | | | |
| 5 | a) | Design a parity generator, where output is 1 for even number of one's and draw the stick diagram for one basic cell. | *CO2* | *PO2* | **10** |
| | b) | Discuss the operation of CMOS dynamic logic. Also discuss the cascading problem of dynamic CMOS logic. | *CO2* | *PO2* | **10** |

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| | | | **OR** | | | |
| | 6 | a) | Illustrate structured design of bus arbitration logic for n-line bus with suitable diagram. | *CO2* | *PO2* | **10** |
| | | b) | Show an arrangement to generate any logic function of two variable A,B by programming the inputs I0-I3 appropriately with 0's and 1's using 4-way multiplexer. | *CO2* | *PO2* | **10** |
| | | | **MODULE - IV** | | | |
| | 7 | a) | Discuss the general arrangements of a 4-bit arithmetic processor. | *CO3* | *PO3* | **10** |
| | | b) | Describe 4x4 barrel shifter with neat diagram. | *CO3* | *PO3* | **10** |
| | | | **OR** | | | |
| | 8 | a) | Describe the architectural issues related to sub system design. | *CO3* | *PO3* | **10** |
| | | b) | Illustrate Two-phase clock generator using D flipflops to generate output frequency of one-quarter of the input frequency. | *CO3* | *PO3* | **10** |
| | | | **MODULE - V** | | | |
| | 9 | a) | Discuss the operation of 3 transistors DRAM Cell and draw its stick diagram. | *CO3* | *PO3* | **10** |
| | | b) | Describe one transistor dynamic memory cell with schematic and stick diagram. | *CO3* | *PO3* | **10** |
| | | | **OR** | | | |
| | 10 | a) | Discuss CMOS pseudo static memory cell and draw its stick diagram. | *CO3* | *PO3* | **10** |
| | | b) | Discuss about optimization and CAD tools for design and simulation of digital logic. | *CO3* | *PO3* | **10** |

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