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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E.   **Semester: III**
Branch: Electronics & Telecommunication Engineering   **Duration: 3 hrs.**
Course Code: 22ET3PCALC   **Max Marks: 100**
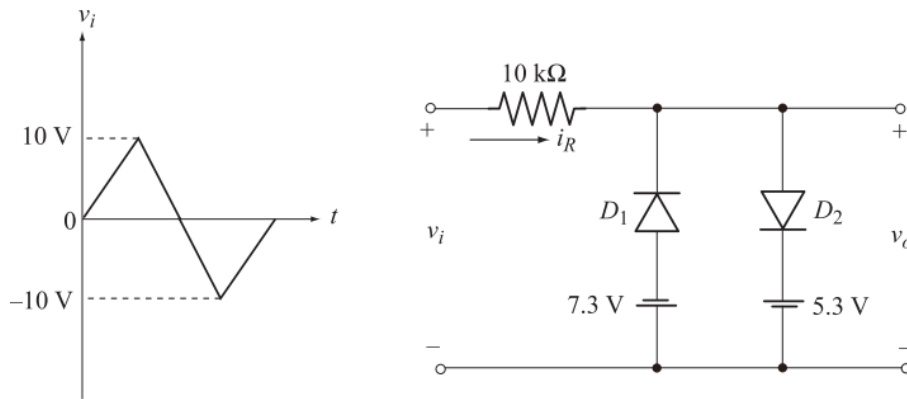**Course: Analog and Linear Circuits**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
                  2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) For the circuit shown in Fig.1, determine the transfer characteristics and sketch the waveform for V_o .   **05**
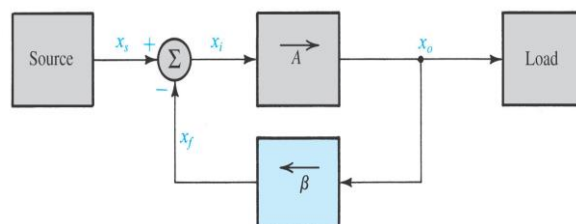

Figure 1

  b) Determine the value of R_c, R_E, R_1 and R_2 for the voltage divider circuit with I_c =10mA, V_{CE} = 12V and V_{cc} =24V. Assume silicon transistor with beta equal to 100.   **07**

  c) What is an operating point? With a neat circuit diagram and relevant expressions explain voltage divider biasing of BJT.   **08**

UNIT - II

2 a) With a neat circuit diagram, waveforms, explain the working of complementary symmetry class B amplifier. Also, derive an expression for conversation efficiency   **08**

  b) Identify the amplifier shown in Figure 2 and enumerate its properties.   **07**

Figure 2

c) Calculate gain, feedback factor, gain with feedback and voltage gain with feedback for the circuit shown in Figure 3 **05**
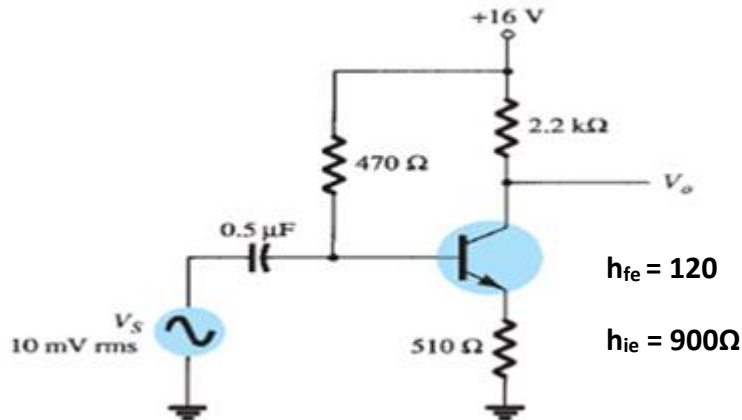

Figure 3

OR

3 a) Derive the **08**

(i) input impedance and voltage gain with feedback for voltage shunt feedback

(ii) output impedance with feedback for current series feedback

b) For a class B amplifier providing a 20V peak signal to a 16Ω load (speaker) and a power supply of $V_{cc} = 30V$, determine the input power, output power and circuit efficiency. **06**

c) For a harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$, and $D_4 = 0.01$, with $I_1 = 4\,A$ and $R_C = 8\,\Omega$, calculate the total harmonic distortion, fundamental power component, and total power. **06**

UNIT - III

4 a) With a neat diagram and i_d - V_{ds} characteristics, explain the operational of n – channel enhancement MOSFET. When **07**

(a) $V_{GS} \leq V_t$
(b) $V_{GS} > V_t\ \&\ V_{DS} < V_{GS} - V_t$
(c) $V_{GS} > V_t\ \&\ V_{DS} \geq V_{GS} - V_t$.

b) For a 0.8μm process technology, for which $t_{ox}= 15nm$ and $\mu_n=550cm^2/V\text{-s}$, find C_{ox}, k'_n and the over drive voltage V_{ov}, required to operate a transistor having W/L =20 in saturation with I_D=0.2mA. What is the minimum value of V_{DS} needed? **05**

c) Derive expression for input resistance, output resistance, voltage gain and overall voltage gain of a common gate MOSFET amplifier. **08**

UNIT - IV

5 a) Discuss the frequency response of a operational amplifier Also explain the Typical frequency response of op-amp 741. **06**

b) Illustrate with the neat diagram and waveforms working of a ZCD. **06**

c) Derive an equation for output voltage of an Instrumentation amplifier using three Opamp with a neat circuit diagram and list its features. **08**

UNIT - V

6 a) Discuss the working of successive approximation ADC with neat sketches. **06**

b) Derive an equation for frequency of square waveform generated by an Astable multivibrator, using 555 timer. Also, explain the working with a neat circuit diagram. **08**

c) Explain the basic principle of a PLL, with a neat block schematic. **06**

OR

7 a) What output voltage would be produced by a D/A converter whose output voltage range is 0V to 10V and whose binary number is
   (i)   01 (for a 2 bit DAC)
   (ii)   1011 (for a 4 bit DAC)
   (iii) 11111001 (for an 8 bit DAC) **06**

b) Describe the principle of working of a weighted resistor DAC with a neat circuit diagram. Mention its limitations. **08**

c) Explain the working of a Flash ADC **06**

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