U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 22ET3PCALC **Max Marks: 100**
Course: Analog and Linear Circuits **Date: 08.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Draw the r_e model for a voltage divider bias configuration and derive expressions for input impedance, output impedance and voltage gain. **08**

b) Determine the levels of I_{CQ} and V_{CEQ} for the voltage divider bias circuit shown in the figure 1. **06**

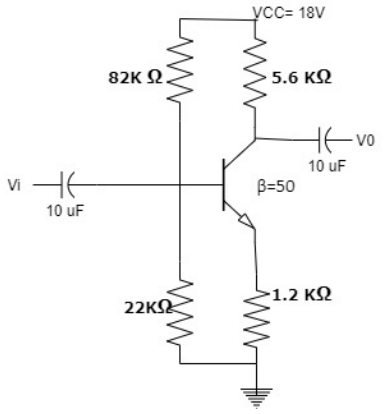

Figure.1

c) Analyze the circuit shown in figure 2 and sketch the input and ouput voltage waveform assuming an ideal diode. (V_i =20sinɷt). **06**

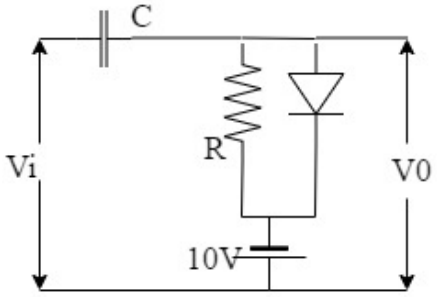

Figure 2

UNIT - II

2 a) With a neat block diagram derive expressions for gain with feedback, input impedance and output impedance for voltage series feedback configuration. **08**

b) Calculate gain, input and output admittance for current series feedback amplifier with A= -300, R_i= 1.5KΩ, R_O= 50KΩ and feedback factor β= -1/15. **06**

c) Calculate the total harmonic distortion for an output signal having fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V. **06**

OR

3 a) Explain the working of class B complementary symmetry push pull amplifier. Also derive an expression for maximum conversion efficiency. **10**

b) It is required to design a class B output stage to deliver an average power of 20Watt to an 8Ω load. The power supply is to be selected such that V_{CC} is about 5V greater than peak output voltage. Determine the supply voltage required, the peak current drawn from each supply, the total supply power and power conversion efficiency. **10**

UNIT - III

4 a) Derive an expression for i) input impedance ii) output impedance iii) voltage gain and overall voltage gain for a common source amplifier with source resistance. **10**

b) Explain the effects of biasing by fixing V_{GS} in a MOSFET with i_D- V_{GS} characteristics. **10**

UNIT - IV

5 a) With a neat circuit diagram describe the working of the circuit which gives the output shown in the figure3 for an input signal V_i =10sinωt **10**

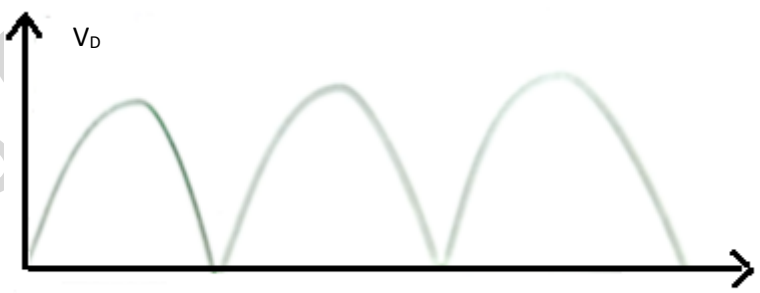

Figure 3

b) Find V_o for the circuit shown in figure 4. **06**

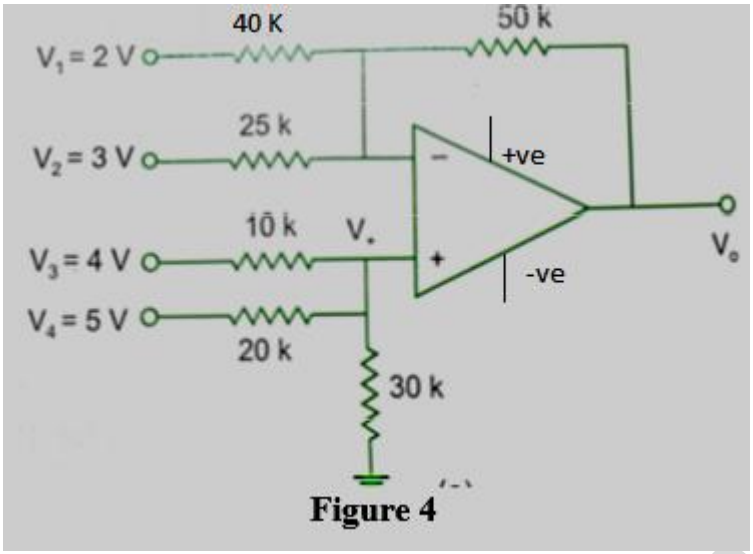

Figure 4

c) Mention the advantages of negative feedback in op-amp **04**

UNIT - V

6 a) With a neat functional diagram describe the working of 555 Timer for monostable operation **10**

b) For the circuit shown in figure 5, determine the value of R_f that should be connected to achieve the following output conditions for R=10KΩ and V_R=10V **10**

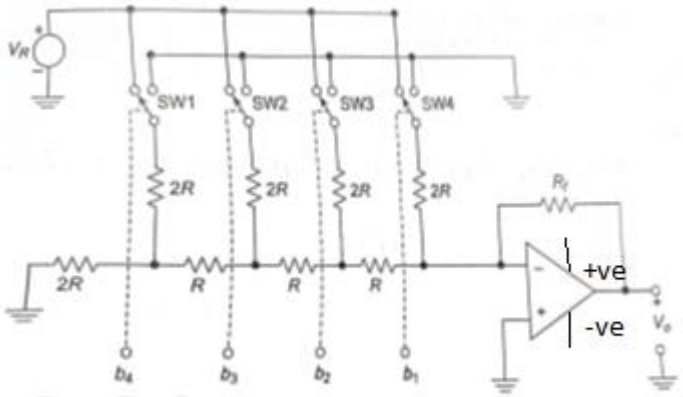

Figure 5

i) The value of LSB at the output is 0.5V
ii) An analog output of 6Vfor a binary input of 1000
iii) The full scale output voltage of 12V
iv) The actual maximum output voltage of 10V

OR

7 a) Describe the basic operation of Phase Locked Loop (PLL) with a neat block diagram. **10**

b) With neat diagram explain the working of dual slope ADC. **10**

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