

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2025 Semester End Make-Up Examinations

Programme: B.E.

Semester: III

Branch: Electronics & Telecommunication Engineering

Duration: 3 hrs.

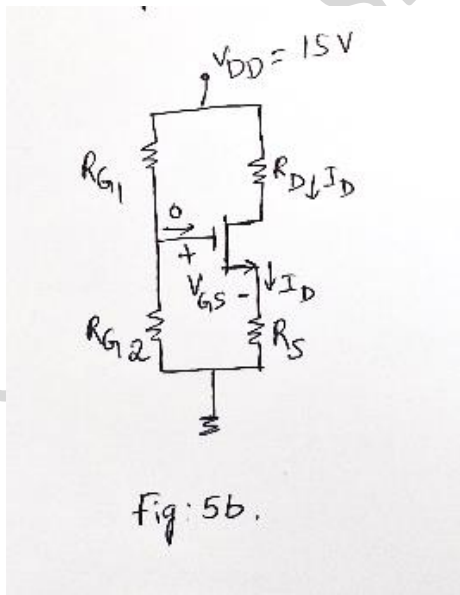
Course Code: 23ET3PCALC

Max Marks: 100

Course: Analog and Linear Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

| Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice. | | | UNIT - I | CO | PO | Marks |
|--|---|----|---|-----|-----|-------|
| | 1 | a) | Design a clipper circuit to clip the negative signal at 2 volts using Series Clipping circuit. | CO1 | | 04 |
| | | b) | Explain the design constraints of classical discrete-circuit biasing arrangement with circuit and relevant equations and explain how R_E provides a negative feedback action to stabilize the bias current. | CO1 | | 08 |
| | | c) | Design the Voltage Divider Bias network of the amplifier to establish a current $I_E = 1 \text{ mA}$, using a power supply of $V_{CC} = +12 \text{ V}$. The transistor is specified to have a nominal β value of 100. | CO1 | | 08 |
| | | | OR | | | |
| | 2 | a) | Derive the expression for i_c and g_m using of Hybrid- π Model of the BJT (consider BJT as voltage controlled current source) | CO1 | | 04 |
| | | b) | Explain with a neat circuits diagram the biasing using a Collector-to-Base Feedback Resistor. Derive the expressions for I_E and V_{CB} | CO1 | | 08 |
| | | c) | Design the circuit of collector to base bias CE amplifier to obtain a dc emitter current of 1 mA, maximum gain, and a $\pm 2\text{-V}$ signal swing at the collector; that is, design for $V_{CE} = +2.3 \text{ V}$. Let $V_{CC} = 10 \text{ V}$ and $\beta = 100$. | CO1 | | 08 |
| | | | UNIT - II | | | |
| | 3 | a) | Derive the expression for gain with feedback using block diagram of general structure of the feedback amplifier. | CO2 | PO1 | 08 |
| | | b) | Explain the following properties of Negative feedback: (a) Gain De-sensitivity (b) Bandwidth Extension (c) Decrease in Non-linear effect (d) Increase in SNR | CO2 | PO1 | 12 |
| | | | OR | | | |

| | | | | | |
|---|----|---|-----|-----|----|
| 4 | a) | Derive the expression of power-conversion efficiency of Class A amplifier with help of a neat circuit diagram and explanation | CO2 | PO1 | 08 |
| | b) | <p>Explain the working of Class B output stage amplifier with help of neat circuit diagram and transfer characteristics.</p> <p>It is required to design a class B output stage to deliver an average power of 20 W to an 8-Ω load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion and allows for including short-circuit protection circuitry. Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.</p> | CO2 | PO1 | 12 |
| | | UNIT - III | | | |
| 5 | a) | Explain the effects of Biasing by Fixing V_{GS} in a MOSFET with i_D - v_{GS} characteristic | CO3 | PO1 | 08 |
| | b) | <p>Design the circuit of Fig. 5b to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $(k_n' W/L) = 1$ mA/V². For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V.</p>  <p>Fig. 5b.</p> | CO3 | PO2 | 08 |
| | c) | Derive the expression for the Signal Current in the Drain Terminal for small signal operation with the help of a neat Conceptual amplifier circuit diagram. | CO3 | PO1 | 04 |
| | | OR | | | |
| 6 | a) | Explain the Biasing by Fixing V_G and Connecting a Resistance in the Source for MOSFET with the help of neat circuit diagrams | CO3 | PO1 | 08 |
| | b) | Find the dc current I_D and DC voltage V_D , g_m , voltage gain for amplifier circuit shown in Fig. 6b. if $v_{gs} = 0.2 \sin \omega t$ volts, find v_d | CO3 | PO2 | 08 |

assuming small-signal approximation holds. Let $V_{DD}=5V$, $R_D=10K\Omega$, $V_t=1V$, $(k_n' W/L) = 20\mu A/V^2$, $V_{GS}=2V$ assume $\lambda=0$.

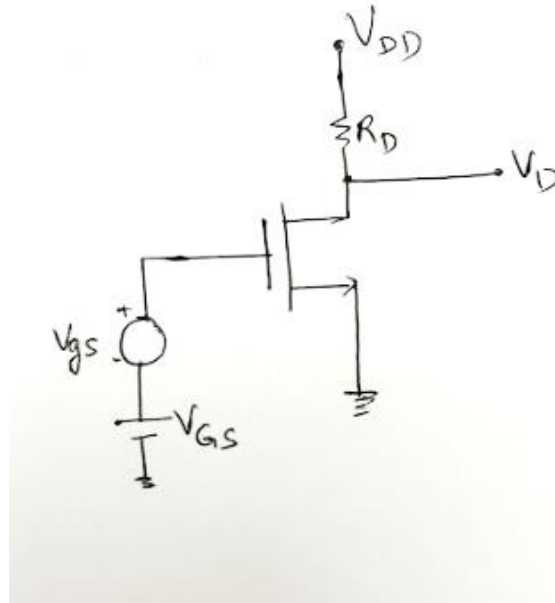


Fig. 6b

- c) Derive the expression for the Voltage Gain of a MOSFET amplifier. Draw the instantaneous waveforms for v_{GS} and v_{DS}

CO3

PO2

04

UNIT - IV

- 7 a) Derive the expression for the closed loop gain of the Inverting and Non-inverting amplifier

CO4

PO1

10

- b) Explain in detail positive and negative wave precision rectifier

CO4

PO1

10

OR

- 8 a) Explain with a neat circuit diagram Instrumentation Amplifier

CO4

PO1

10

- b) Explain the following with a neat circuit diagram

CO4

PO1

10

- a. Comparator
- b. Virtual ground

UNIT - V

- 9 a) Explain the ADC using Successive-approximation method with help neat circuit diagram.

CO3

PO1

10

- b) Explain the DAC using R-2R ladder with help neat circuit diagram

CO3

PO1

10

OR

- 10 a) Explain the internal block diagram of 555 timer

CO3

PO1

10

- b) Explain with neat circuit the operation of Mono stable Multivibrator

CO3

PO1

10
