U.S.N.										

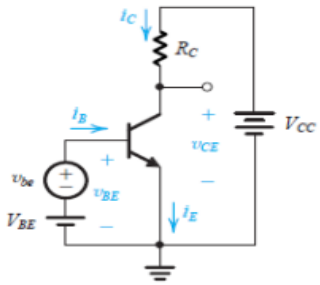
B.M.S. College of Engineering, Bengaluru-560019

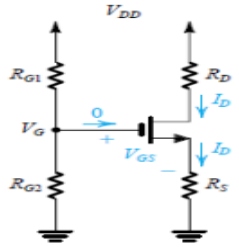
Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 23ET3PCALC **Max Marks: 100**
Course: Analog and Linear Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Explain the design constraint of classical discrete-circuit biasing arrangement with circuit and relevant equations and also explain how does R_E provide a negative feedback action to stabilize the bias current.	CO1,2	PO1, 2,3	**08**
	b)	Calculate the voltage gain of the circuit shown in Fig. 1b for v_{be} = 0.005 cosωt V, also find $v_C(t)$ and $i_B(t)$, if V_{BE} is adjusted to yield a dc collector current of 1 mA, V_{CC} = 15 V, R_C = 5 kΩ, and β = 100.  Fig. 1b	CO1,2	PO1,2,3	**08**
	c)	Calculate the expected range of I_E if the transistor used has β in the range of 50 to 150. R_1= 80K ohm, R_2= 40K ohm, R_E= 3K ohm.	CO1,2	PO1,2,3	**04**
		UNIT - II			
2	a)	Prove the following properties of Negative feedback: (a) Gain De-sensitivity (b) Bandwidth Extension	CO1,2	PO1,2,3	**10**
	b)	Derive the expression of Gain, Input-Resistance, and Output-resistance for voltage amplifier with the help of a neat circuit diagram and explanation.	CO1,2	PO1,2,3	**10**
		OR			
3	a)	Derive the expression of power-conversion efficiency of Class A amplifier with the help of a neat circuit diagram and explanation.	CO1,2	PO1,2,3	**10**

		b)	Derive the expression of power-conversion efficiency of Class B amplifier with the help of a neat circuit diagram and explanation.	*CO1,2*	*PO1,2,3*	**10**
			UNIT - III			
	4	a)	Explain the effects of Biasing by Fixing V_{GS} in a MOSFET with i_D–V_{GS} characteristic.	*CO1,2*	*PO1,2,3*	**08**
		b)	Design the circuit of Fig. 3b to establish a dc drain current I_D = 0.5 mA. The MOSFET is specified to have Vt = 1 V and (kn′ W ⁄ L) = 1 mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume λ = 0). Use a power-supply V_{DD} = 15 V.Ig=1uA.  Fig.3b	*CO1,2*	*PO1,2,3*	**08**
		c)	Explain with a neat circuit diagram the Biasing of MOSFET using a Drain-to-Gate Feedback Resistor.	*CO1,2*	*PO1,2,3*	**04**
			UNIT - IV			
	5	a)	Explain positive and negative half wave precision rectifier with the help of neat circuit diagrams and relevant waveforms.	*CO3,4*	*PO1,2,3*	**10**
		b)	Explain with a neat circuit diagram Instrumentation Amplifier Using Transducer Bridge.	*CO3.4*	*PO1,2,3*	**10**
			UNIT – V			
	6	a)	Explain the DAC using R-2R ladder with the help of a neat circuit diagram.	*CO3.4*	*PO1,2,3*	**10**
		b)	Explain the internal block diagram of 555 timer with a neat diagram.	*CO3,4*	*PO1,2,3*	**10**
			OR			
	7	a)	Explain the ADC using the Successive-approximation method with the help of a neat circuit diagram.	*CO3,4*	*PO1,2,3*	**10**
		b)	Explain with a neat circuit diagram the working of a Monostable Multivibrator.	*CO3,4*	*PO1,2,3*	**10**

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