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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: IV**

Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 23ET4PCHDL **Max Marks: 100**

Course: Verilog HDL

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Write the need of HDL? Explain the history of Verilog.	CO1	PO1	**06**
	b)	Describe the types or levels of Verilog HDL descriptions.	CO1	PO1	**06**
	c)	Explain the top-down and bottom-up design methodologies with block diagram.	CO1	PO1	**08**
		OR			
2	a)	Draw the typical design flow chart for designing VLSI IC circuits and write the importance of HDLs.	CO1	PO1	**06**
	b)	Discuss the trends in HDL.	CO1	PO1	**06**
	c)	Write the Design and stimulus block of 4-bit ripple carry counter with Verilog HDL.	CO2	PO2	**08**
		UNIT - II			
3	a)	Define a module and explain the components of Verilog module.	CO1	PO1	**06**
	b)	Illustrate the different lexical conventions that are used in Verilog HDL.	CO1	PO1	**06**
	c)	Discuss the compiler directives that are used in Verilog.	CO1	PO1	**08**
		OR			
4	a)	Discuss the different Data Types used in Verilog with examples.	CO1	PO1	**06**
	b)	Describe the system tasks that are used in Verilog.	CO1	PO1	**06**
	c)	Write the Verilog module of full adder using half adder. Illustrate the connection of ports by order and name with respect to full adder using half adder.	CO2	PO2	**08**
		UNIT - III			
5	a)	Explain and/or & buf/not built in primitives with example.	CO2	PO2	**06**

		b)	Discuss the Different types of operators used in verilog with example.	*CO2*	*PO2*	**06**
		c)	Define Instance. Write the Gate level modeling for 4-to-1 line Multiplexer with stimulus block.	*CO2*	*PO2*	**08**
			OR			
	6	a)	Illustrate rise, fall and turn-off delays with example.	*CO2*	*PO2*	**06**
		b)	Write the dataflow Verilog module for 4 to 1 line Multiplexer using ternary operator.	*CO2*	*PO2*	**06**
		c)	Write the dataflow Verilog module for 4-bit full adder with carry look ahead adder.	*CO2*	*PO3*	**08**
			UNIT - IV			
	7	a)	Write the Verilog module for 4 to 2 line Priority Encoder, give the highest priority to MSB bit.	*CO3*	*PO2*	**06**
		b)	Compare initial with always block. Illustrate with example.	*CO3*	*PO2*	**06**
		c)	Discuss Regular delay control and Intra-assignment delay control statements with example.	*CO3*	*PO3*	**08**
			OR			
	8	a)	Write the Behavioral Verilog module for 2 to 1 line multiplexer and verify the design with test bench module.	*CO3*	*PO3*	**06**
		b)	Compare blocking with non-blocking assignment statements. Illustrate with example.	*CO3*	*PO2*	**06**
		c)	Explain the loop statements, Illustrate with example.	*CO3*	*PO2*	**08**
			UNIT - V			
	9	a)	Synthesize the following code: if(s) y=a; else y=b. Derive the RTL diagram.	*CO4*	*PO5*	**06**
		b)	Discuss the impact of logic synthesis.	*CO4*	*PO5*	**06**
		c)	Describe the mapping of case statement with and without storage to RTL schematic by taking suitable examples.	*CO4*	*PO9*	**08**
			OR			
	10	a)	Define synthesis and explain synthesis design flow from RTL to gates.	*CO4*	*PO5*	**06**
		b)	Describe the modeling tips for logic synthesis with examples.	*CO4*	*PO5*	**06**
		c)	Write the Verilog module to synthesize the function to calculate Y=2*X+3, where X is 0 to 4. Derive the RTL Diagram.	*CO4*	*PO9*	**08**

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