U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2023 Semester End Main Examinations

Programme: B.E. **Semester: IV**

Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 19ET4PCVLD **Max Marks: 100**

Course: VLSI Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Along with proper diagrams, explain the fabrication of n - MOS transistor	**08**
	b)	Write the stick diagram and mask layout for 2-input CMOS NOR gate	**06**
	c)	Discuss Lambda based design rules	**06**

OR

2	a)	Discuss the CMOS inverter in detail, along with the respective diagrams and tabulations	**08**
	b)	Along with proper diagrams, explain the working of an n-channel Enhancement MOSFET and discuss modes as well as the regions	**06**
	c)	Analyze with relevant diagrams the CMOS Twin Tub process	**06**

UNIT - II

3	a)	Implement and analyze a 3 I/P Dynamic CMOS NOR logic. Also implement its stick diagram.	**08**
	b)	Explain and implement a Bi-CMOS NAND logic structure.	**06**
	c)	Analyze the Transmission gate and Tristate Inverter.	**06**

UNIT - III

4	a)	Derive the inverter delays for the following using appropriate terminologies: i) CMOS inverter ii) nMOS inverter	**08**
	b)	Derive expressions for Rise and Fall time delays.	**06**
	c)	Define sheet resistance and area capacitance with appropriate terminologies.	**06**

UNIT - IV

5	a)	Implement and analyze the operation of a Carry Skip Adder.	**10**
	b)	Implement and analyze the operation of Braun Array multiplier.	**10**

OR

6	a)	Implement and analyze the operation of a Manchester Carry chain adder.	**10**
	b)	Implement and analyze the operation of a Wallace tree multiplier.	**10**

UNIT - V

7	a)	Explain the operation of 3T dynamic RAM cell and 1T dynamic memory cell.	**10**
	b)	Discuss any five practical testability methodologies.	**10**

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