U.S.N.											

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: IV**

Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

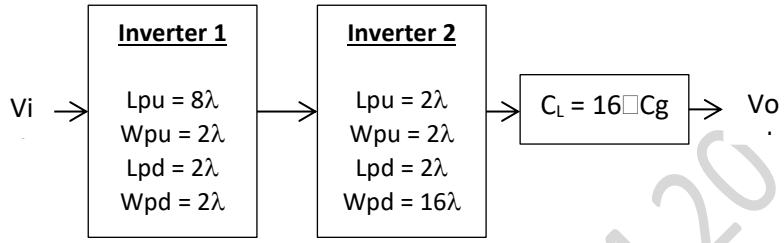
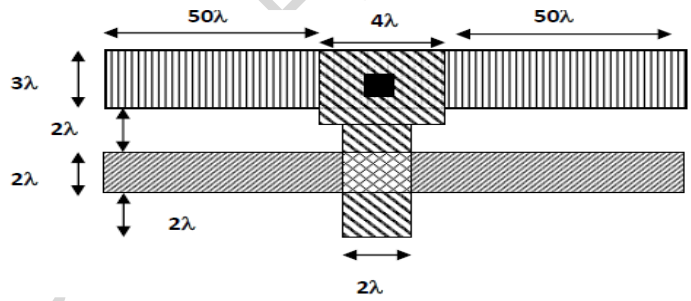
Course Code: 19ET4PCVLD **Max Marks: 100**

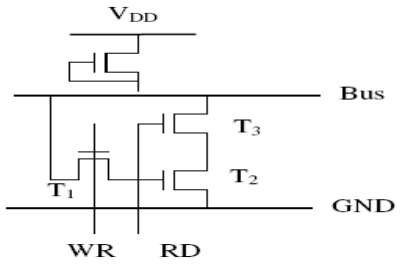
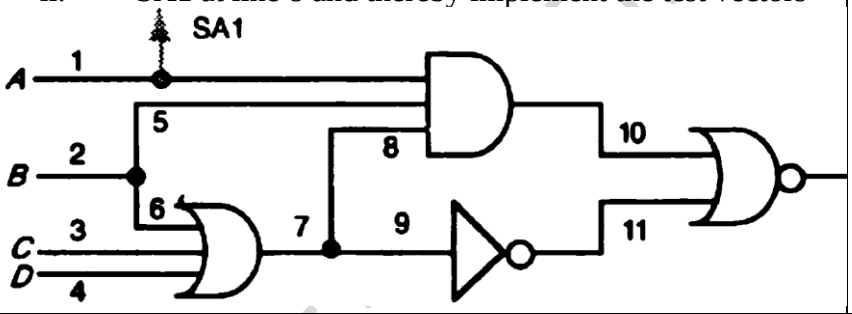
Course: VLSI Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define Moore's first law with an appropriate graph and thereby explain its implication.	CO1		**04**
	b)	With neat sketches, analyze the nMOS fabrication technique. Clearly describe the various masking operations performed.	CO1		**08**
	c)	Design and implement the logic function, Y = (A+B) . C using minimum number of transistors. Use CMOS technology for implementation and thereby sketch the stick diagram.	CO3	PO3	**08**
		OR			
2	a)	Compare CMOS and Bipolar technologies.	CO1		**04**
	b)	Analyze with relevant diagrams and masking operations, the p-well fabrication process.	CO2	PO1	**08**
	c)	Using minimum number of transistors, design the logic function Y = (A+BC) and thereby implement the same using monochrome layout diagram.	CO2	PO1	**08**
		UNIT - II			
3	a)	Design a circuit for the expression Y = $\overline{A+BC}$ through CVSL technology and explain the advantages of CVSL technology.	CO3	PO3	**10**
	b)	Design a RS latch dynamic CMOS circuit and analyze its working principle and thereby sketch its stick diagram.	CO3	PO3	**10**
		OR			
4	a)	Design a 3-input OR gate using C^2MOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	CO3	PO3	**10**
	b)	Design a 4:1 Mux using Transmission gate and analyze its working principle. Also sketch the stick diagram for a 2:1 Mux circuit.	CO3	PO3	**10**

			UNIT - III			
	5	a)	Derive the expressions for rise – time estimation and fall – time estimation of a CMOS inverter with relevant terminologies.	*CO2*	*PO1*	**06**
		b)	Explain the basic architectural guidelines considered in VLSI design.	*CO1*		**04**
		c)	Two nMOS inverters are cascaded as shown in Fig below. Calculate the delay in terms of τ. $C_1 = 4\square Cg$ at the output of first inverter, hence analyze: (i) The delay if $\tau = 0.4$ ns (ii) If due to connecting wires, the stray capacitance increases by $4\square Cg$, what is the delay time? 	*CO3*	*PO4*	**10**
			OR			
	6	a)	Prove that the total time constant is 0.7 ns for a CMOS inverter and 0.5 ns for an nMOS inverter. Use appropriate terminologies and equivalent circuits for your analysis.	*CO3*	*PO2*	**10**
		b)	Determine the total capacitance between the following area and substrate in the figure given below. Consider 5μm technology for your calculations. 	*CO3*	*PO2*	**10**
			UNIT - IV			
	7	a)	Design and analyze the following: i. 4-bit combinational shifter ii. 4 X 4 barrel shifter	*CO3*	*PO3*	**10**
		b)	Design and analyze with relevant diagrams a Manchester carry chain adder and also write the stick diagram for a 1-bit Manchester chain.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Design and analyze the following: i. 4 bit SISO dynamic register ii. 4 X 4 cross bar switch	*CO3*	*PO3*	**10**

		b)	Design and analyze with relevant diagrams a Serial-Parallel multiplier. Consider an example for your analysis.	*CO3*	*PO3*	**10**
			UNIT - V			
	9	a)	Identify the memory device in figure below and thereby explain its operation.  	*CO2*	*PO1*	**03**
		b)	Analyze the practical design issues of testability with respect to the following: i. Controllability and Observability ii. Gated Clocks iii. Redundant Logic	*CO2*	*PO1*	**07**
		c)	For the circuit given below in figure below consider a i. SA1 at line1 and thereby implement the test vectors ii. SA1 at line 8 and thereby implement the test vectors  	*CO3*	*PO4*	**10**
			OR			
	10	a)	Analyze the following practical design issues in VLSI testing environment: i. Use of Bus structures ii. Self – Reset Logic iii. BILBO testing	*CO4*	*PO2*	**10**
		b)	Implement and analyze the following memory cells. Sketch the equivalent stick diagrams. i. 3T Dynamic RAM cell ii. Pseudo static memory cell	*CO4*	*PO2*	**10**

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