U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: IV**

Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 19ET4PCVLD **Max Marks: 100**

Course: VLSI Design **Date: 15.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Explain the operation and V-I characteristics of the Enhancement mode n-MOS transistor with necessary diagrams.		**08**
	b)	With neat diagrams discuss the nMOS fabrication process mentioning all the mask used in the process.		**08**
	c)	Draw a stick diagram for 2 i/p CMOS AND gate.		**04**

OR

2	a)	Explain with neat diagrams n-well based CMOS fabrication process mentioning all the masks used in the process.		**08**
	b)	Draw stick diagram and layout diagram for Y = (AB+CD)' using CMOS design style		**08**
	c)	Discuss various λ-based design rules used in design of layout.		**04**

UNIT - II

3	a)	Implement the given Boolean expression Y =(A(B+C)+(D.E))' in the following logic structures:		**08**
		(i) Pseudo –nMOS logic (ii) CVSL		

b) Explain the working operation of Domino CMOS logic considering the example of a 2 input OR gate. Also implement its stick diagram. **08**

c) Use transmission gate to implement 4:1 Multiplexer using 2:1 Multiplexer **04**

UNIT - III

4 a) Derive the expression for rise time and fall time of a CMOS inverter. Also, show that for symmetric operations Wp = 2.5 Wn **08**

b) Implement the following: **08**

i) Combinational Bidirectional Shifter.
ii) 4X4 Barrel Shifter.

c) Discuss the general consideration taken care in the design of CMOS Subsystem **04**

UNIT - IV

5 a) Explain the working of Wallace tree Multiplier with a neat diagram. **10**

b) Explain Manchester carry chain adder with diagram. **10**

OR

6 a) Explain Carry Select adders with a neat diagram. **10**

b) With a neat diagram explain Modified Booth's Multiplier. **10**

UNIT - V

7 a) Explain 3 transistor dynamic and one transistor dynamic RAM memory cells with a neat circuit diagram and stick diagram. **10**

b) Analyze the following with relevant diagrams: **10**

i) Ground rules for design (any four)
ii) Sensitized path testing.

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