U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: V**
Branch: Electronics & Telecommunication Engg **Duration: 3 hrs.**
Course Code: 22ET5PE1DD **Max Marks: 100**
Course: DIGITAL SYSTEM DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Write a Verilog code for any five gates in different modules.	*CO1*		**10**
	b)	Draw the state level diagram and develop the Verilog for a non-overlapping Mealy state machine which produces output as '1' if the input bit stream is "1101" with neat indentation.	*CO2*	*PO1*	**10**
		OR			
2	a)	What is FSM? With a neat block diagram explain the different types of FSMs?	*CO1*		**10**
	b)	Mention any four Verilog operators and illustrate the same using data flow modeling.	*CO1*		**10**
		UNIT - II			
3	a)	Realize CMOS Inverter using MOS switches and write the Verilog description for the same.	*CO2*	*PO1*	**10**
	b)	For the following Verilog constructs what is the interpretation of the synthesis tools to translate for gate-level representation. i)The if statement ii)The case statement iii)The always statement Write a simple Verilog code to justify the above statements.	*CO2*	*PO1*	**06**
	c)	Which are the Verilog operators supported for synthesis (any 4).	*CO1*		**04**
		UNIT - III			
4	a)	Explain the different types of PLDs.	*CO1*		**10**
	b)	What is FPGA? Explain the different components of FPGA.	*CO1*		**10**
		UNIT - IV			
5	a)	Design and write Verilog code to implement the functionality of 4-bit Carry Look Ahead Adder.	*CO2*	*PO1*	**10**

		b)	Design and write Verilog code to implement multiplication of two, 2-bit binary numbers.	*CO2*	*PO1*	**10**
			OR			
	6	a)	Design and write Verilog code to implement the functionality of 1-bit Full Adder using Data flow modeling.	*CO3*	*PO3*	**10**
		b)	Illustrate the concept of division for two 4-bit numbers	*CO2*	*PO1*	**10**
			UNIT - V			
	7	a)	What are SM charts and explain the components of SM charts.	*CO1*		**10**
		b)	Explain the derivation of SM Charts for any digital system.	*CO1*		**10**

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