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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

July 2024 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 22ET5PE1DD **Max Marks: 100**
Course: Digital System Design

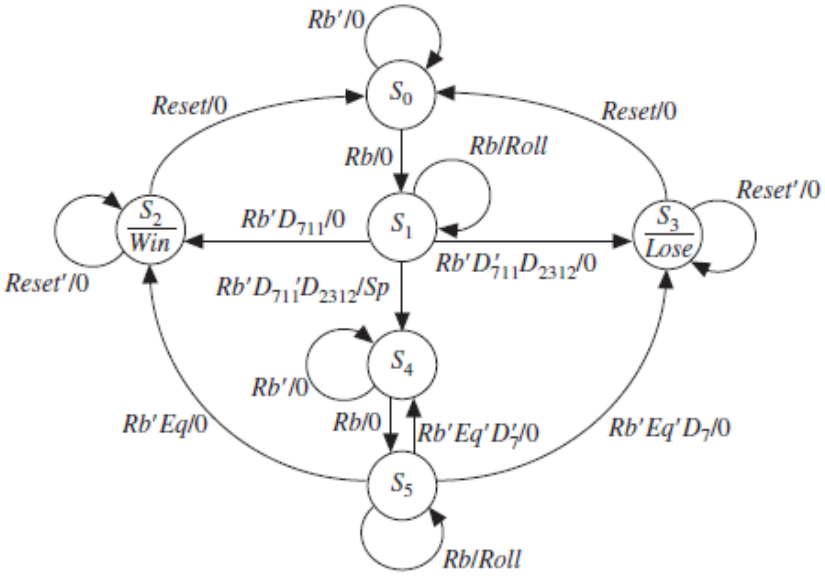
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Analyze with relevant diagram the HDL design flow.	*CO2*	*PO1*	**07**
	b)		Analyze the following directives: i. `define ii. `include	*CO2*	*PO1*	**03**
	c)		Design and implement a data flow description in Verilog HDL for Negative Edge-Triggered D-flipflop with clear circuit. Supplement your code with appropriate example and circuit diagram.	*CO3*	*PO3*	**10**
			OR			
2	a)		Analyze the value levels and strength levels supported by Verilog HDL to model the functionality of real hardware.	*CO2*	*PO1*	**07**
	b)		If X, Y and Z are three unsigned variables with X = 1111 0000, Y = 0101 1101 and Z=00000000, determine the values for the following: (i) X && Z (ii) ! Y (iii) Y << 1	*CO2*	*PO1*	**03**
	c)		Design a 4 bit Ripple Subtractor using Full adders. Write a Gate level Verilog HDL code to implement the same.	*CO3*	*PO3*	**10**
			UNIT - II			
3	a)		Write a switch level modeled Verilog HDL program to implement a two input CMOS Flipflop. Also verify your output using an appropriate stimulus code.	*CO2*	*PO1*	**06**
	b)		Write a switch level modeled Verilog HDL program to implement a two input CMOS NOR gate. Also verify your output using an appropriate stimulus code.	*CO2*	*PO1*	**06**

		c)	Develop synthesized logic output and the gate level diagram for the following code:
			module magnitude_comparator(A_gt_B, A_lt_B, A_eq_B, A, B) ;
			output A_gt_B, A_lt_B, A_eq_B;
			input [3:0] A, B;
			assign A_gt_B = (A > B);
			assign A_lt_B = (A < B);
			assign A_eq_B = (A == B);
			endmodule
				CO2	*PO1*	**08**

			UNIT - III			
	4	a)	Using a CPLD, implement a Parallel Adder with Accumulator. Support your solution with relevant circuit diagram and equations	*CO1*		**10**
		b)	The following state table is implemented using a ROM and two D flip-flops (falling edge triggered): $Q_1\ Q_2$ | $Q_1 + Q_2 +$ (X=0) | $Q_1 + Q_2 +$ (X=1) | Z (X=0) | Z (X=1) 00 | 01 | 10 | 0 | 1 01 | 10 | 00 | 1 | 1 10 | 00 | 01 | 1 | 0 i. Draw the block diagram. ii. Write Verilog code that describes the system. Assume that the ROM has a delay of 10 ns and each flip-flop has a propagation delay of 15 ns.	*CO2*	*PO1*	**10**
			UNIT - IV			
	5	a)	Implement and write the Verilog HDL code for a 2-digit BCD adder with relevant block diagram.	*CO2*	*PO1*	**10**
		b)	Write a Verilog Behavioral model code for a 32-Bit Divider.	*CO2*	*PO1*	**10**
			OR			
	6	a)	Design and write a Verilog HDL code sequential traffic light controller for the intersection of street "A" and street "B." Each street has traffic sensors, which detect the presence of vehicles approaching or stopped at the intersection. Sa = 1 means a vehicle is approaching on street "A," and Sb = 1 means a vehicle is approaching on street "B." Street "A" is a main street and has a	*CO3*	*PO3*	**12**

			green light until a car approaches on "B." Then the lights change, and "B" has a green light.			
		b)	Write a Verilog Behavioral model code for a 4 × 4 Binary Multiplier.	*CO2*	*PO1*	**08**
			UNIT - V			
	7	a)	Consider the following State diagram of a Dice game controller:  Write a Verilog Behavioral model code for the same.	*CO4*	*PO4*	**14**
		b)	With relevant SM Charts, analyse the concept of Serially Linked State Machines	*CO1*		**06**

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