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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## June / July 2025 Semester End Main Examinations

**Programme: B.E.** **Semester: V**

**Branch: Electronics & Telecommunication Engineering** **Duration: 3 hrs.**

**Course Code: 23ET5PE1DD / 22ET5PE1DD** **Max Marks: 100**

**Course: DIGITAL SYSTEM DESIGN**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

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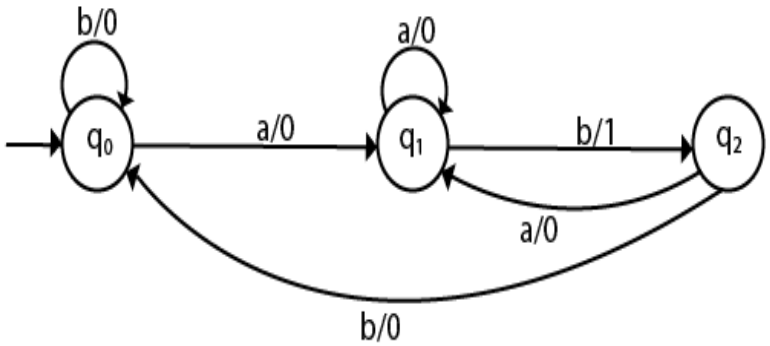
**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | UNIT - I | CO | PO | Marks |
|---|---|---|---|---|---|
| 1 | a) | Design a Full Adder using a suitable decoder and hence describe the behavior in Verilog HDL | CO3 | PO3 | **06** |
| | b) | Design a BCD to Excess-3 code converter using sequential logic with Verilog | CO3 | PO3 | **08** |
| | c) | Analyze the following operations and design using Verilog HDL<br>**control** \| **operation**<br>00 \| Transfer<br>01 \| >> 1<br>10 \| >>> 2<br>11 \| << 3 | CO3 | PO3 | **06** |
| | | **OR** | | | |
| 2 | a) | Convert the following Mealy FSM to Moore FSM<br>  | CO2 | PO2 | **06** |
| | b) | Write a Verilog model of the Mealy FSM described by the state diagram with a test bench | CO3 | PO3 | **06** |

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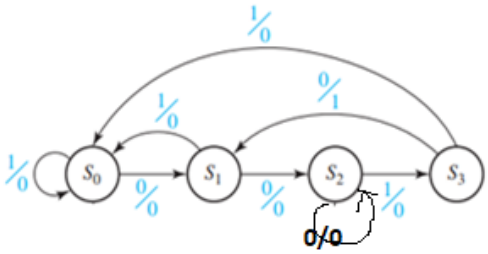
|---|---|---|---|---|---|---|
| | | |  | | | |
| | | c) | Design a synchronous counter using D-FFs for the sequence 0, 1, 2, 4, 6, 0 and hence describe the behavior in Verilog HDL | *CO3* | *PO3* | **08** |
| | | | **UNIT - II** | | | |
| | 3 | a) | Explain Synthesis process with flow chart | *CO1* | *PO1* | **04** |
| | | b) | Design a switch level diagram for the function **Y =** $\overline{(\mathbf{A}+\mathbf{B})(\mathbf{C}+\mathbf{D})\mathbf{E}}$ and hence describe the behavior in Verilog | *CO2* | *PO2* | **06** |
| | | c) | For the following code obtain gate level synthesis<br>**module example (a, y);**<br>**input [2:0]a;**<br>**output [3:0]y;**<br>**reg y;**<br>**always@ (a)**<br>**begin**<br>**if (a<3'b101)**<br>**y=2*a +5;**<br>**end**<br>**endmodule** | *CO3* | *PO3* | **10** |
| | | | **OR** | | | |
| | 4 | a) | Design a D-FF using minimum number of transistors and hence describe the behavior in Verilog HDL | *CO3* | *PO3* | **06** |
| | | b) | Design a 2-to-1 multiplexer using bufif0 and bufif1 gates and hence describe the Verilog behavior | *CO2* | *PO2* | **04** |
| | | c) | Analyze the following Verilog process and give the circuit generated by the code 8M<br>**module syn (clk,clr,Dout, Din,load);**<br>**input clk,clr;**<br>**input [3:0] Din;**<br>**output reg [3:0] Dout;**<br>**always @ (posedge clk or posedge clr)**<br>**begin**<br>**if (clr == 1'b1) Dout <= 4'b0;**<br>**else if (load ==1'b1) Dout <=Din;**<br>**end**<br>**endmodule** | *CO3* | *PO3* | **10** |
| | | | **UNIT - III** | | | |
| | 5 | a) | List the steps for designing a digital system with FPGA | *CO1* | *PO1* | **04** |

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|---|---|---|---|---|---|---|
| | | b) | Realize a 2-bit binary counter using Xilinx 3000 series OR Xilinx 4000 series device | *CO2* | *PO2* | **08** |
| | | c) | Realize the following functions using PLA<br>**F1 (A,B,C,D) = ∑m(2,3,5,7,8,9,10,11,13,15)**<br>**F2 (A,B,C,D) = ∑m(2,3,5,6,7,10,11,14,15)**<br>**F3 (A,B,C,D) = ∑m(6,7,8,9,13,14,15)** | *CO2* | *PO2* | **08** |
| | | | **OR** | | | |
| | 6 | a) | Briefly explain the operation of ALTERA 7000 series CPLD | *CO1* | *PO1* | **08** |
| | | b) | Realize the following functions using a suitable PAL<br>$Q_1^+ = A' B Q_1 + A' B' Q_2'$<br>$Q_2^+ = A Q_2 + B' Q_1'$ | *CO2* | *PO2* | **08** |
| | | c) | With a neat diagram explain the operation of I/O block in 3000 series FPGA | *CO1* | *PO1* | **04** |
| | | | **UNIT - IV** | | | |
| | 7 | a) | Design and draw the gate level diagram and hence write the Verilog code for 2-bit X 2- bit Combinational Array Multiplier. Also write the stimulus block | *CO3* | *PO3* | **10** |
| | | b) | With a neat block diagram explain the operation of serial adder with accumulator | *CO1* | *PO1* | **05** |
| | | c) | Draw the state graph for binary divider which divides 8-bit dividend to 4-bit divisor | *CO2* | *PO2* | **05** |
| | | | **OR** | | | |
| | 8 | a) | Draw the state graph and hence write a Verilog code for 4-bit X 4-bit unsigned Binary multiplier | *CO3* | *PO3* | **08** |
| | | b) | Write a Verilog code for 4-bit carry look ahead adder | *CO3* | *PO3* | **04** |
| | | c) | Write state graph and Verilog description of a traffic light controller for the intersection of street A and street B with the following conditions:<br>i. When A is green, it remains green at least 50sec, and then the lights changes only when a vehicle approaches on B.<br>ii. When B is green, it remains in green at least 40sec, and then the lights change back unless there is a vehicle on street B and none on street A. | *CO3* | *PO3* | **08** |
| | | | **UNIT - V** | | | |
| | 9 | a) | Draw an SM chart for half adder | *CO2* | *PO2* | **05** |
| | | b) | Explain the concept of linked state machines | *CO1* | *PO1* | **05** |
| | | c) | Draw an SM chart and hence write a Verilog code for 4-bit multiplier control network | *CO3* | *PO3* | **10** |

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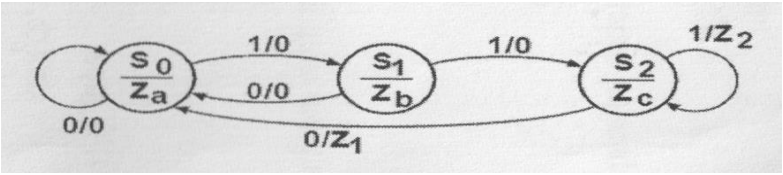
|---|---|---|---|---|---|---|
| | | | **OR** | | | |
| | 10 | a) | Realize SM chart and hence write Verilog code for Dice game controller | *CO3* | *PO3* | **10** |
| | | b) | Explain the concept of microprogramming | *CO3* | *PO1* | **05** |
| | | c) | Convert the following state diagram to state machine chart.   | *CO3* | *PO2* | **05** |

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