U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 23ET5PE1DD / 22ET5PE1DD **Max Marks: 100**

Course: DIGITAL SYSTEM DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	PO	Marks
		UNIT - I			
1	a)	Explain the structure of Verilog module for full adder using half adder.	CO1	PO1	**06**
	b)	Illustrate Unary, Binary and Ternary operators are used in Verilog with example.	CO1	PO1	**06**
	c)	Write the Verilog module for 4 to 1 line Multiplexer using dataflow and Behavioral modeling. Compare with execution.	CO1	PO2	**08**
		OR			
2	a)	Compare Mealy with Moore FSM Designs.	CO1	PO1	**06**
	b)	Discuss the importance of Data Types used in Verilog HDL. Illustrate with example.	CO1	PO1	**06**
	c)	Design and Implement FSM for BCD to Excess-3 code Convertor using DFF.	CO3	PO3	**08**
		UNIT - II			
3	a)	What is logic synthesis? Describe the Synthesis design Flow with neat flowchart.	CO3	PO1	**06**
	b)	Construct 2 to 1 line Multiplexer using CMOS switches and write the switch level modeling.	CO2	PO2	**06**
	c)	Draw the circuit for NOR gate using transistors and write Verilog code using CMOS switches with test bench to verify the design.	CO2	PO2	**08**
		OR			
4	a)	Write the switch level modeling for $Y = (A + BC)'$. Verify the design with stimulus block.	CO2	PO2	**06**

		b)	Discuss the impact of logic synthesis and trade-off between area and time.	*CO2*	*PO1*	**06**
		c)	Write the behavioral model to calculate the function y=2x+3, where x is 0 to 3 and derive the RTL schematic.	*CO3*	*PO3*	**08**
			UNIT - III			
	5	a)	Illustrate the classification of popular or major Programmable Logic Devices with neat block-bricks.	*CO1*	*PO1*	**06**
		b)	Write the functional table for full adder and implement sum and carry expressions using Programmable Array Logic (PAL).	*CO3*	*PO3*	**06**
		c)	Draw the architecture of Complex Programmable Logic Devices (CPLDs) and explain the operation.	*CO2*	*PO1*	**08**
			OR			
	6	a)	Compare the following: i) PLA with PAL. ii) CPLD with FPGA.	*CO2*	*PO1*	**06**
		b)	Realize the following Boolean expressions using 4×5×3 Programmable Logic Array (PLA). F1 =∑m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15) F2 =∑m(2, 3, 5, 6, 7, 10, 11, 14, 15) F3 =∑m(6, 7, 8, 9, 13, 14, 15)	*CO3*	*PO3*	**06**
		c)	Draw the architecture of Field-Programmable Gate Arrays (FPGAs) and explain the operation.	*CO2*	*PO1*	**08**
			UNIT - IV			
	7	a)	Write the block diagram of a BCD to 7-Segment Display Decoder and write the behavioral Verilog module.	*CO3*	*PO3*	**06**
		b)	Draw the Block Diagram for Binary parallel divider and illustrate the operation with example.	*CO2*	*PO2*	**06**
		c)	Design and write Verilog Description of a 4-Bit Carry Look-Ahead Adder.	*CO3*	*PO3*	**08**
			OR			
	8	a)	Illustrate the addition of two BCD numbers and write the Verilog code.	*CO3*	*PO3*	**06**
		b)	Draw the Block Diagram for Binary Multiplier and illustrate the operation with example.	*CO2*	*PO2*	**06**
		c)	Write the State Graph for Traffic Light Controller and write the Verilog Code for Traffic-Light Controller.	*CO3*	*PO3*	**08**
			UNIT - V			
	9	a)	Explain the principal components of an SM charts with neat block views. Draw the SM chart for the equation *Y=A+A'BC.*	*CO1*	*PO1*	**06**

		b)	Draw and explain SM Charts for Serially Linked State Machines.	*CO2*	*PO2*	**06**
		c)	Write the SM Chart for Binary multiplier and write the Verilog code for the multiplier controller.	*CO3*	*PO3*	**08**
			OR			
	10	a)	Illustrate Parallel and Serial form SM blocks with flowchart.	*CO2*	*PO2*	**06**
		b)	For the Dice game based on the following rules, draw the SM chart and develop the behavioral Verilog code. I) After the 1st roll of the dice the player wins if the sum is 7 or 11. The player loses if the sum is 2, 3 or 12. Otherwise, the sum the player obtained on the 1st roll is referred to as a point and he/she must roll the dice again. II) On the 2nd or subsequent roll of the dice, the player wins if the sum equals the point, and he/she loses if the sum is 7. Otherwise, the player must roll again until he/she finally wins or loses. Write a test -bench for the dice game problem to test the game components.	*CO3*	*PO3*	**14**

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