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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 19ET5PE2VH **Max Marks: 100**

Course: Verilog HDL **Date: 07.03.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	What are the trends followed in HDLs? Explain in brief.	**06**
	b)	Explain the typical steps involved in VLSI IC design flow.	**06**
	c)	Explain 4 different levels of design abstractions used in Verilog HDL.	**08**

UNIT - II

2	a)	Explain integer, real, and time datatypes with an example for each.	**06**
	b)	Explain any 4 system tasks with an example for each.	**08**
	c)	What are the various components of Verilog module? Explain in brief.	**06**

UNIT - III

3	a)	Define rise, fall, and turn-off delays.	**06**
	b)	Explain the gate instantiation of logic gates `bufif' and `notif' with an example for each.	**04**
	c)	Write a Verilog code for a 4×1 multiplexer using gate-level description. Also write the test bench code.	**10**

OR

4	a)	How to specify delays in continuous assignment statements? Explain with an example.	**06**
	b)	Explain with an example the syntax of various Verilog reduction operators.	**06**
	c)	Write a Verilog code for 4-bit carry look ahead adder using dataflow description.	**08**

UNIT - IV

5	a)	Explain two structured procedures used in Verilog with an example for each.	**06**
	b)	Differentiate between blocking and non-blocking assignment statements with an example.	**06**

c) Write a Verilog code for 8×1 multiplexer using i) case statement ii) if/else-if statement. **08**

OR

6 a) Describe the NMOS, PMOS, and CMOS switch modelling elements with an example. **06**

b) Design and also write the switch level description for the following Boolean equations. **10**

i) $Z = \overline{AB + CD + E}$

ii) $W = \overline{(A + B)C + D}$

c) List out differences between regular and resistive switches. **04**

UNIT - V

7 a) Explain the logic synthesis flow from RTL to gates. **10**

b) What is logic synthesis? Explain the impact of logic synthesis. **10**

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