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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

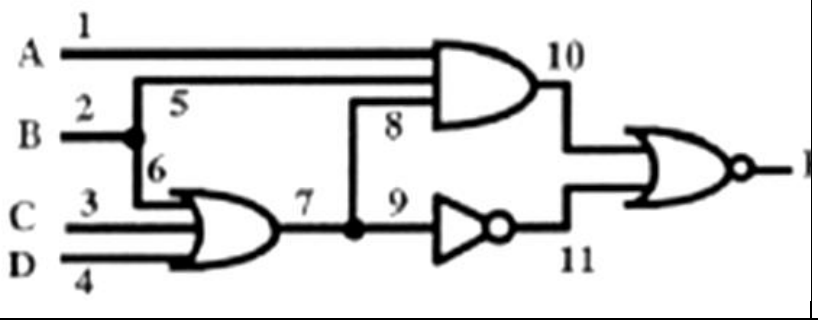
Course Code: 23ET5PCFLI **Max Marks: 100**

Course: FUNDAMENTALS OF VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define and analyze with a neat graph the Moore's First law.	CO1	-	**06**
	b)	Design and implement the expression 3 input NAND gate using minimum number of transistors. Use CMOS technology for implementation and thereby sketch: i. Monochrome layout diagram ii. Stick diagram	CO3	PO3	**14**
		OR			
2	a)	Compare CMOS and Bipolar technologies.	CO1	-	**06**
	b)	Explain the process of pMOS fabrication with relevant diagrams and masking steps.	CO1	-	**08**
	c)	Explain λ based design rules for fabrication.	CO1	-	**06**
		UNIT - II			
3	a)	Design and analyze the operation of a Cascode Voltage Switch Logic 2 input AND / NAND gate.	CO3	PO3	**10**
	b)	Design a 2 input NOR gate using Tri-state CMOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	CO3	PO3	**10**
		OR			
4	a)	Design a RS latch dynamic CMOS circuit and analyze its working principle and thereby sketch its stick diagram.	CO3	PO3	**10**
	b)	Design a 3 input NOR gate using Pseudo nMOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	CO3	PO3	**10**

			UNIT - III			
	5	a)	Derive the expressions for rise – time estimation and fall – time estimation of a CMOS inverter with relevant terminologies.	*CO3*	*PO2*	**12**
		b)	Explain the basic architectural guidelines considered in VLSI design.	*CO1*	-	**08**
			OR			
	6	a)	Analyze and implement a 1 bit magnitude comparator circuit using 4:1 multiplexer as leaf cells.	*CO2*	*PO1*	**08**
		b)	Prove that the total time constant is 0.7 ns for a CMOS inverter and 0.5 ns for an nMOS inverter. Use appropriate terminologies and equivalent circuits for your analysis.	*CO3*	*PO2*	**12**
			UNIT - IV			
	7	a)	Design and analyze the following: i. 4-bit combinational shifter ii. 4X4 Barrel shifter	*CO2*	*PO1*	**10**
		b)	Design and analyze with relevant diagrams a Carry select adder and also write the stick diagram for a 1-bit Manchester chain.	*CO2*	*PO1*	**10**
			OR			
	8	a)	Design and analyze the following: i. 4 bit SISO dynamic register ii. 4X 4 cross bar switch	*CO2*	*PO1*	**10**
		b)	Design and analyze with relevant diagrams a Serial-Parallel multiplier. Consider an example for your analysis.	*CO2*	*PO1*	**10**
			UNIT - V			
	9	a)	Analyze the practical design issues of testability with respect to the following: i. Controllability and Observability ii. Gated Clocks	*CO1*	-	**08**
		b)	Consider the circuit diagram shown in figure below. If L1 is SA1, analyze and interpret its test vectors considering the three testing stages of DFT principle. 	*CO3*	*PO3*	**12**

			OR			
	10	a)	Implement and analyze the following memory cells. Sketch the equivalent stick diagrams. i. 3T Dynamic RAM cell ii. Pseudo static memory cell	*CO1*	-	**12**
		b)	Analyze the practical design issues of testability with respect to the following: (i) Bus Structure (ii) BILBO testing	*CO1*	-	**08**

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