U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

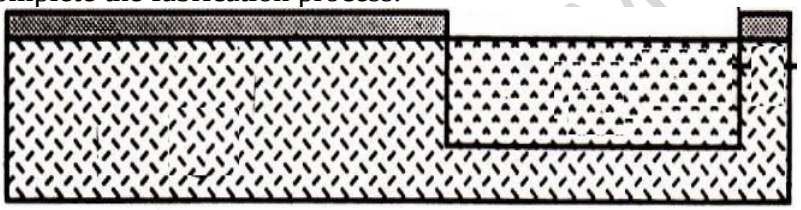
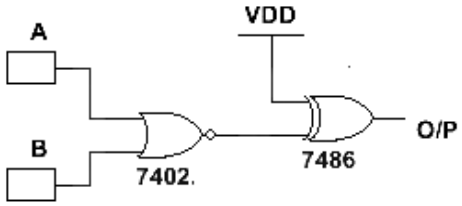
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

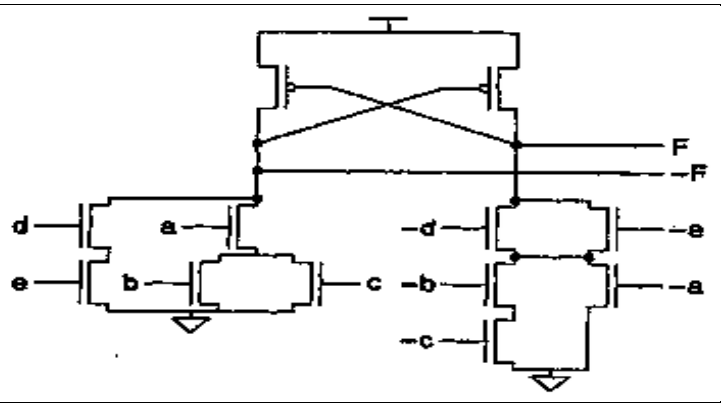
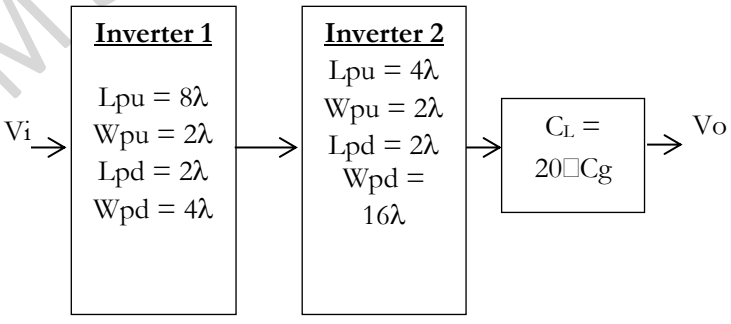
Course Code: 23ET5PCFLI **Max Marks: 100**

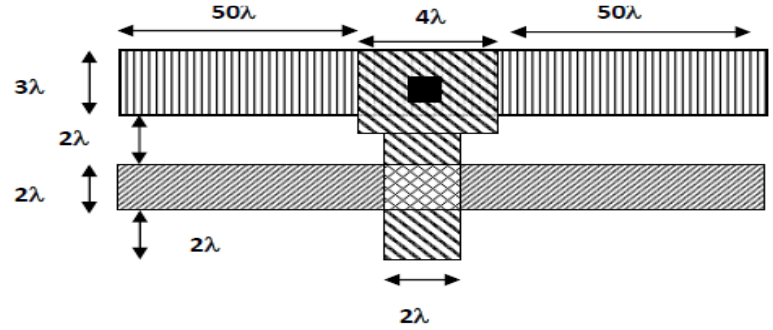
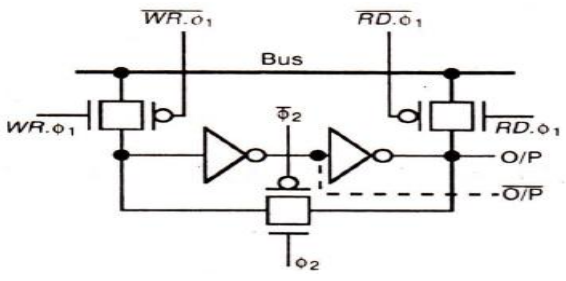
Course: FUNDAMENTALS OF VLSI

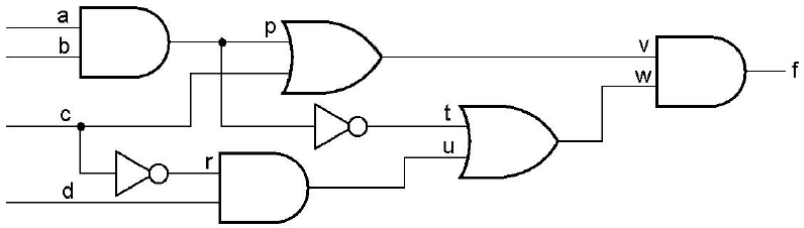
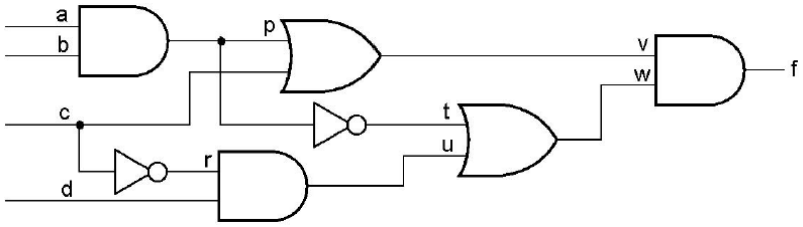
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Considering the initial process of fabrication given below, complete the fabrication process. 	*CO2*	*PO1*	**10**
	b)		Design and implement a CMOS circuit for the expression Y = A+BC using minimum number of transistors. Also implement its Stick diagram.	*CO3*	*PO3*	**10**
			OR			
2	a)		Design and implement the circuit shown below using minimum number of transistors. Use CMOS technology for implementation and thereby sketch the Monochrome layout diagram. 	*CO3*	*PO3*	**10**
	b)		Analyze with relevant diagrams and masking operations, the CMOS twin tub fabrication process.	*CO1*	-	**10**
			UNIT - II			
3	a)		Design a 3 input OR gate using C^2MOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	*CO3*	*PO3*	**14**
	b)		Interpret the output of the following circuit shown below and write the output expression and its stick diagram.	*CO3*	*PO2*	**06**

						
			OR			
4	a)		Design, analyze and implement a Dynamic CMOS circuit for a 3 input NOR gate with minimum number of transistors. Also sketch the stick diagram for the same.	*CO3*	*PO3*	**14**
	b)		Design a 4:1 Mux using Transmission gate and write its functional table. Also sketch the stick diagram for a 2:1 Mux circuit.	*CO3*	*PO3*	**06**
			UNIT - III			
5	a)		Derive the expressions for rise – time estimation and fall – time estimation of a CMOS inverter with relevant terminologies.	*CO2*	*PO1*	**05**
	b)		Analyze the basic architectural guidelines considered in VLSI design.	*CO1*	-	**05**
	c)		Two nMOS inverters are cascaded as shown in Fig below. Calculate the delay in terms of τ. If $C_1 = 8\square Cg$ at the output of first inverter, determine: (i) The delay if $\tau = 0.6$ ns? (ii) If due to connecting wires, the stray capacitance increases by $8\square Cg$, what is the delay time? (iii) Implement the stick diagram of the nMOS inverter. 	*CO3*	*PO2*	**10**
			OR			
6	a)		Starting from the nMOS inverter characteristics, derive the expression for Z_{pu}/Z_{pd} of an nMOS inverter driven by another nMOS inverter. Also analyze different nMOS inverter implementations.	*CO2*	*PO1*	**10**

		b)	Determine the total capacitance between the following area and substrate in the figure given below. Consider 5μm technology for your calculations.  	*CO3*	*PO2*	**10**
			UNIT - IV			
	7	a)	Design a 4 – bit Combinational shifter and briefly analyze its functioning with an appropriate truth table. Also write the stick diagram for 1 – bit inverting register.	*CO3*	*PO2*	**05**
		b)	Implement and analyze a 4 – bit serial – parallel multiplier circuit.	*CO1*	-	**05**
		c)	Derive an expression for the computation time 'T' for the Carry Select Adder and thereby derive the minimum T for a 128 bit carry select adder, with 16ns delay through every adder cell and 2ns delay through the multiplexer. Determine number of blocks and number of adder cells in each block for achieving minimum T.	*CO2*	*PO1*	**10**
			OR			
	8	a)	Design and analyze the operation of a 4 –bit Barrel shifter.	*CO1*	-	**05**
		b)	Implement and analyze the working of a 24 – bit Carry skip adder. Also derive the optimization technique used for the carry skip adder.	*CO1*	-	**05**
		c)	Consider the example of $(127)_{10}$ X $(126)_{10}$ and thereby implement the multiplication using: i. Traditional Booth multiplier ii. Modified Booth multiplier Complete the process of multiplication using appropriate encoding tables for both the cases.	*CO3*	*PO2*	**10**
			UNIT - V			
	9	a)	Identify the memory logic in the circuit given below and thereby analyze its working principle.  	*CO2*	*PO1*	**06**

		b)	The logic network shown below has inputs a, b, c, d and output f. Find all test vectors which can be used to find a **SA1** for signal **u**.  	*CO3*	*PO3*	**14**
			OR			
	10	a)	Analyze the practical design issues of testability with respect to the following: i. Controllability and Observability ii. Gated Clocks	*CO1*	-	**06**
		b)	The logic network shown below has inputs a, b, c, d and output f. Find all test vectors which can be used to find a **SA1** for signal **t**.  	*CO3*	*PO3*	**14**

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