U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

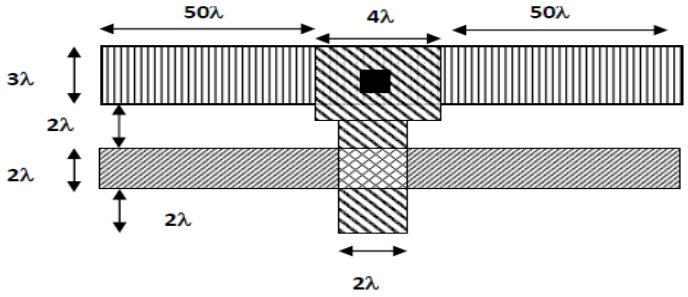
January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 22ET6PCVLS **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define Moore's first law with an appropriate graph and thereby explain its implication.	CO1	PO1	**04**
	b)	With neat sketches, analyze the nMOS fabrication technique. Clearly describe the various masking operations performed.	CO1	PO1	**08**
	c)	Design and implement the logic function, Y = (A+B).C using minimum number of transistors. Use CMOS technology for implementation and thereby sketch the stick diagram.	CO1	PO1	**08**
		OR			
2	a)	Compare CMOS and Bipolar technologies.	CO1	PO1	**04**
	b)	Analyze with relevant diagrams and masking operations, the CMOS twin tub fabrication process.	CO1	PO1	**08**
	c)	Using minimum number of transistors, design the logic function Y = (A+BC) and thereby implement the same using monochrome layout diagram.	CO1	PO1	**08**
		UNIT - II			
3	a)	Design and analyze the operation of a Cascode Voltage Switch Logic 2-input AND / NAND gate.	CO2	PO2	**06**
	b)	Design a 3-input OR gate using C^2MOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	CO2	PO2	**08**
	c)	Design a 4:1 Mux using Transmission gate and analyze its working principle. Also sketch the stick diagram for a 2:1 Mux circuit.	CO2	PO2	**06**
		OR			
4	a)	Draw and explain the operation of 2- input NAND gate in Bi-CMOS logic	CO2	PO2	**10**
	b)	What is a pass transistor? Design a pass transistor network that implements the function **F = A B C + A B' C' + A' B' C + A' B C'**	CO2	PO2	**10**

			UNIT - III			
	5	a)	Prove that the total time constant is 0.7 ns for a CMOS inverter and 0.5 ns for an nMOS inverter. Use appropriate terminologies and equivalent circuits for your analysis.	*CO3*	*PO2*	**10**
		b)	Determine the total capacitance between the following area and substrate in the figure given below. Consider 5μm technology for your calculations. 	*CO3*	*PO2*	**10**
			OR			
	6	a)	Determine the expressions for rise and fall times of a CMOS inverter	*CO3*	*PO2*	**10**
		b)	Design a 4-bit bidirectional shifter.	*CO3*	*PO2*	**08**
			UNIT - IV			
	7	a)	Design and implement a 4 X 4 Barrel shifter circuit and also analyze its advantages over a traditional crossbar switch. Substantiate your reply with diagrams of both the switches.	*CO3*	*PO2*	**10**
		b)	Implement and analyze the working of a 24 – bit Carry skip adder. Also explain the optimization technique used for the carry skip adder.	*CO3*	*PO2*	**10**
			OR			
	8	a)	Design and analyze a 4 – bit adder circuit using the principle of Manchester carry chain. Also write the stick diagram of a single bit Manchester carry chain.	*CO3*	*PO2*	**10**
		b)	Design and analyze with relevant diagram a Serial parallel multiplier.	*CO3*	*PO2*	**10**
			UNIT - V			
	9	a)	Analyze the following practical design issues in VLSI testing environment: i. Controllability and Observability ii. Self – Reset Logic	*CO4*	*PO2*	**10**
		b)	Implement and analyze the following memory cells. Sketch the equivalent stick diagrams. i. 3T Dynamic RAM cell ii. 1T memory cell	*CO4*	*PO2*	**10**
			OR			
	10	a)	Briefly explain Ground rules for successful VLSI design	*CO4*	*PO1*	**08**
		b)	Draw the CMOS circuit and stick diagram for pseudo-static memory cell	*CO4*	*PO1*	**12**

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