U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

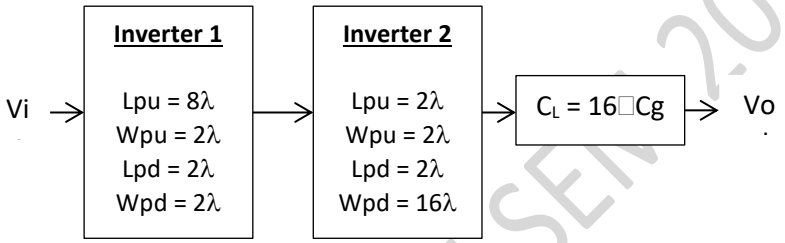
June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 22ET6PCVLS **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Draw and explain the DC characteristics of CMOS inverter	CO1	PO1	**08**
	b)	With neat sketches, explain the fabrication process of nMOS Transistor	CO1	PO1	**08**
	c)	Design a CMOS diagram for the function $\mathbf{Y = \overline{(A + B)C}}$ and hence describe the same using stick diagram	CO1	PO1	**04**
		OR			
2	a)	With neat sketches, explain the Twin-tub fabrication process of CMOS Transistor	CO1	PO1	**08**
	b)	Draw and explain the DC characteristics of nMOS inverter	CO1	PO1	**08**
	c)	Design a CMOS diagram for the function $\mathbf{Y = \overline{(A + B)(C + D)}}$ and hence describe the same using stick diagram	CO1	PO1	**04**
		UNIT - II			
3	a)	Design 4:1 multiplexer using transmission gates and also write the stick diagram for 2:1 mux.	CO2	PO2	**08**
	b)	Draw and explain the operation of 2- input NAND gate in Bi-CMOS logic	CO2	PO2	**06**
	c)	What is a pass transistor? Design a pass transistor network that implements the function **F = A B C + A B' C' + A' B' C + A' B C'**	CO2	PO2	**06**
		OR			
4	a)	Design a circuit for the expression $Y = \overline{A + BC}$ through CVSL technology and explain the advantages of CVSL technology.	CO3	PO3	**10**
	b)	Design a RS latch dynamic CMOS circuit and analyze its working principle and thereby sketch its stick diagram.	CO3	PO3	**10**

			UNIT - III			
	5	a)	Determine the expressions for rise and fall times of a CMOS inverter	*CO3*	*PO2*	**06**
		b)	Design a 4-bit bidirectional shifter	*CO3*	*PO2*	**08**
		c)	Explain Switch logic and Gate logic with an example	*CO3*	*PO2*	**06**
			OR			
	6	a)	Prove that the total time constant is 0.7 ns for a CMOS inverter and 0.5 ns for an nMOS inverter. Use appropriate terminologies and equivalent circuits for your analysis.	*CO3*	*PO2*	**10**
		b)	Two nMOS inverters are cascaded as shown in Fig below. Calculate the delay in terms of τ. $C_1 = 4\square Cg$ at the output of first inverter, hence analyze: (i) The delay if $\tau = 0.4$ ns (ii) If due to connecting wires, the stray capacitance increases by $4\square Cg$, what is the delay time? 	*CO3*	*PO4*	**10**
			UNIT - IV			
	7	a)	Design 1-bit adder and draw its circuit using CMOS logic	*CO3*	*PO2*	**06**
		b)	List the important guidelines to design a system	*CO3*	*PO2*	**06**
		c)	With a neat circuit diagram explain the operation of 4-bit Wallace tree multiplier	*CO3*	*PO2*	**08**
			OR			
	8	a)	Design and analyze with relevant diagrams a Manchester carry chain adder and also write the stick diagram for a 1-bit Manchester chain.	*CO3*	*PO2*	**10**
		b)	With a neat circuit diagram explain the operation of 4-bit Booth multiplier	*CO3*	*PO2*	**10**
			UNIT - V			
	9	a)	Briefly explain Ground rules for successful VLSI design	*CO4*	*PO1*	**06**
		b)	Define Controllability and Observability	*CO4*	*PO1*	**06**
		c)	Draw the CMOS circuit and stick diagram for pseudo-static memory cell	*CO4*	*PO1*	**08**
			OR			
	10	a)	Analyze the following practical design issues in VLSI testing environment: i. Gated clocks ii. Self – Reset Logic	*CO4*	*PO2*	**10**

			iii. Use of multiplexers			
		b)	Implement and analyze the following memory cells. Sketch the equivalent stick diagrams. i. 3T Dynamic RAM cell ii. Pseudo static memory cell	*CO4*	*PO2*	**10**

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