U.S.N.										

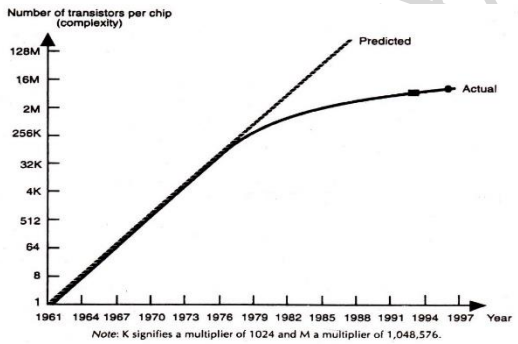
B.M.S. College of Engineering, Bengaluru-560019

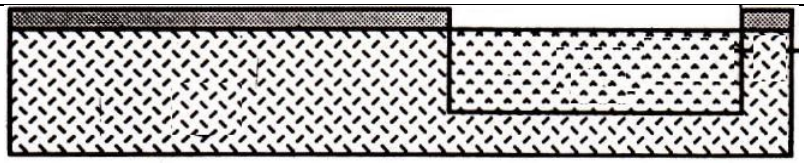
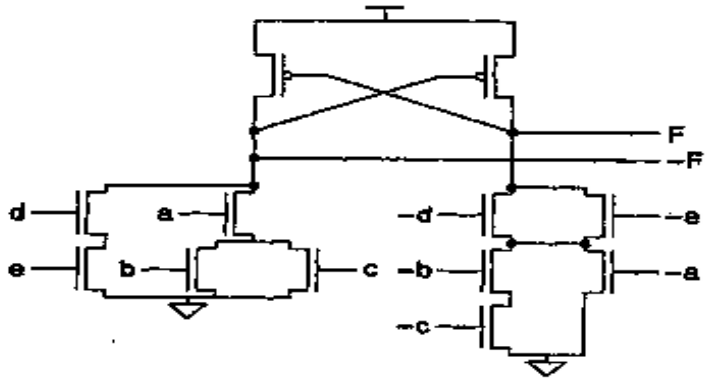
Autonomous Institute Affiliated to VTU

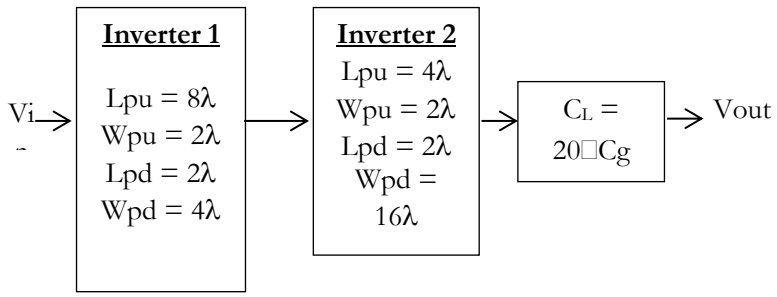
October 2024 Supplementary Examinations

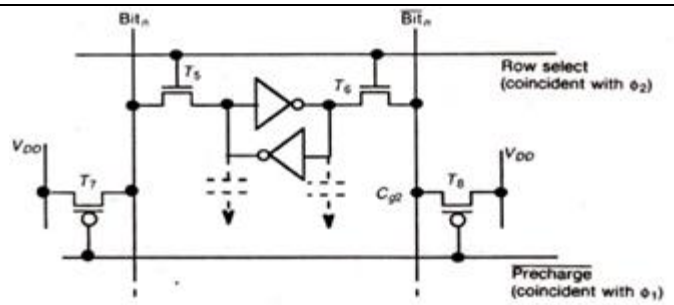
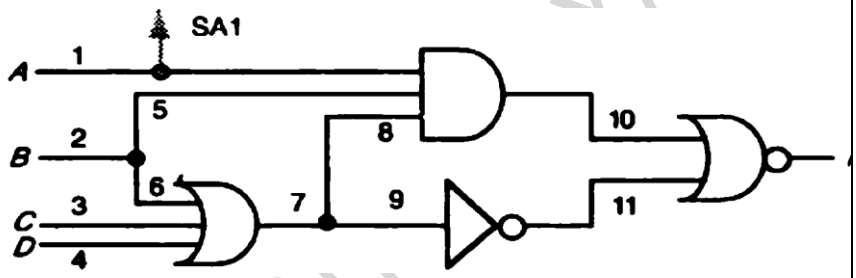
Programme: B.E. **Semester: VI**
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**
Course Code: 22ET6PCVLS **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	CO	PO	Marks
	1	a)	Identify the graph given below in ***Fig.1.1*** and analyze its implications.  ***Fig.1.1***	*CO1*	*PO1*	**05**
		b)	Analyze with relevant diagrams and masking operations, the CMOS twin tub fabrication process.	*CO1*	*PO1*	**05**
		c)	Design and implement the expression Y = $\overline{(A+B)C}$ using minimum number of transistors. Use CMOS technology for implementation and thereby sketch: i. Monochrome layout diagram ii. Stick diagram	*CO1*	*PO1*	**10**
			OR			
	2	a)	Compare CMOS and Bipolar technologies.	*CO1*	*PO1*	**05**
		b)	Considering the initial process of fabrication given below in ***Fig.2.1,*** complete the fabrication process.	*CO1*	*PO1*	**05**

			 *Fig.2.1*			
		c)	Design and implement the expression Y=P+QR Use CMOS technology for implementation and thereby sketch: i. Monochrome layout diagram ii. Stick diagram	*CO1*	*PO1*	**10**
			UNIT - II			
	3	a)	Interpret the output of the following circuit in ***Fig. 3.1*** and write the output expression and its stick diagram.  *Fig. 3.1*	*CO2*	*PO1*	**05**
		b)	Design a 4:1 Mux using Transmission gate and analyze its working principle. Also sketch the stick diagram for a 2:1 Mux circuit.	*CO2*	*PO1*	**05**
		c)	Design a 3 input OR gate using C^2MOS logic and analyze its working principle. Also sketch the stick diagram for the circuit.	*CO2*	*PO1*	**10**
			UNIT - III			
	4	a)	Derive the expressions for rise – time estimation and fall – time estimation of a CMOS inverter with relevant terminologies.	*CO3*	*PO2*	**05**
		b)	Analyze the basic architectural guidelines considered in VLSI design.	*CO3*	*PO2*	**05**
		c)	Two nMOS inverters are cascaded as shown in Fig4.1 below. Calculate the delay in terms of τ. If $C_1 = 8$□Cg at the output of first inverter, determine: (i) The delay if $\tau = 0.6$ ns	*CO3*	*PO2*	**10**

			(ii) If due to connecting wires, the stray capacitance increases by 8□Cg, what is the delay time? (iii) Implement the stick diagram of the nMOS inverter.  ***Fig 4.1***			
			UNIT - IV			
	5	a)	Design a 4 – bit Combinational shifter and briefly analyze its functioning with an appropriate truth table. Also write the stick diagram for 1 – bit inverting register.	***CO3***	***PO2***	**05**
		b)	Implement and analyze a 4 – bit serial – parallel multiplier circuit.	***CO3***	***PO2***	**05**
		c)	Derive an expression for the computation time 'T' for the Carry Select Adder and thereby derive the minimum T for a 128 bit carry select adder, with 16ns delay through every adder cell and 2ns delay through the multiplexer. Determine number of blocks and number of adder cells in each block for achieving minimum T.	***CO3***	***PO2***	**10**
			OR			
	6	a)	Design and analyze the operation of a 4 –bit Barrel shifter.	***CO3***	***PO2***	**05**
		b)	Implement and analyze the working of a 24 – bit Carry skip adder. Also derive the optimization technique used for the carry skip adder.	***CO3***	***PO2***	**05**
		c)	Consider the example of $(126)_{10}$ X $(127)_{10}$ and thereby implement the multiplication using: i. Traditional Booth multiplier ii. Modified Booth multiplier Complete the process of multiplication using appropriate encoding tables for both the cases.	***CO3***	***PO2***	**10**
			UNIT - V			
	7	a)	Identify the memory logic in the circuit given below in ***Fig.7.1*** and thereby analyze its working principle.	***CO4***	***PO4***	**05**

			 ***Fig.7.1***			
	b)	Analyze the practical design issues of testability with respect to the following: i. Controllability and Observability ii. Gated Clocks	***CO4***	***PO2***	**05**
	c)	For the circuit given below in ***Fig.7.2*** below consider a i. SA1 at line1 and thereby implement the test vectors ii. SA1 at line 8 and thereby implement the test vectors  ***Fig.7.2***	***CO4***	***PO4***	**10**

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