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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 22ET7PE3AD **Max Marks: 100**

Course: ASIC DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Explain with relevant diagram the Cell based ASIC structure.	CO1	PO1	**06**
	b)	Explain with relevant diagram the structured gate array	CO1	PO1	**06**
	c)	Explain with relevant diagrams the difference between PLD and FPGA.	CO1	PO1	**08**
		OR			
2	a)	Explain with relevant diagrams the difference between Channeled Gate array and Channelless gate array.	CO1	PO1	**08**
	b)	Explain the design steps for an ASIC.	CO1	PO1	**06**
	c)	Explain the importance of ASIC cell libraries.	CO1	PO1	**06**
		UNIT - II			
3	a)	Write a Verilog HDL code for an 8 bit conditional sum adder.	CO2	PO2	**06**
	b)	Design and implement a Brent Kung CLA.	CO2	PO2	**08**
	c)	Derive an expression for estimating the propagation delay of a logic cell.	CO2	PO2	**06**
		OR			
4	a)	Design and implement a data-path Carry Propagate adder.	CO2	PO2	**06**
	b)	With relevant diagram, implement and analyze a Dadda multiplier.	CO2	PO2	**07**
	c)	Compute the delay involved in implementing the function Z as a multistage AOI logic $Z(A_1, A_2, B_1, B_2, C) = NOT(NAND(A_1, A_2)\ AOI21(B_1, B_2, C\ )))$ Assume $P_{inv} = 1$, $q_{inv} = 1.7$, $r = 1.5$	CO2	PO2	**07**
		UNIT - III			
5	a)	With a neat diagram, explain the Xilinx XC3000 architecture.	CO3	PO1	**08**

		b)	Explain the concept of EPROM technology with relevant diagrams.	*CO3*	*PO1*	**06**
		c)	With a neat diagram, explain the Altera FLEX architecture.	*CO3*	*PO1*	**06**
			OR			
	6	a)	With a neat diagram, explain the Xilinx XC5200 CLB and LC.	*CO3*	*PO1*	**08**
		b)	Explain the concept of metal-metal antifuse technology with relevant diagrams.	*CO3*	*PO1*	**06**
		c)	With a neat diagram, explain the ACT 1 architecture.	*CO3*	*PO1*	**06**
			UNIT - IV			
	7	a)	With a neat diagram, explain the CMOS output buffer characteristics.	*CO3*	*PO1*	**08**
		b)	With a neat diagram, explain the concept of supply bounce.	*CO3*	*PO1*	**06**
		c)	With a neat diagram, explain the concept of metastability.	*CO3*	*PO1*	**06**
			OR			
	8	a)	Considering an appropriate circuit diagram, explain the significance of Elmore's constant and Elmore's delay.	*CO3*	*PO1*	**08**
		b)	With a neat diagram, explain the importance of clamp diodes in determining the CMOS output buffer characteristics.	*CO3*	*PO1*	**06**
		c)	With a neat diagram, explain the importance of noise margins.	*CO3*	*PO1*	**06**
			UNIT - V			
	9	a)	Consider a 4-bit latch and thereby sketch its: i. Schematic from gate level primitives ii. Four instances of cell DLAT iii. Vectored instance of DLAT	*CO3*	*PO2*	**10**
		b)	Explain the hierarchical nature of an EDIF file.	*CO3*	*PO1*	**10**
			OR			
	10	a)	Consider a 16-bit latch and thereby sketch its: i. Schematic for 4 instances of 4-bit latch ii. Four multiple instances of 4-bit latch	*CO3*	*PO2*	**10**
		b)	With relevant diagrams, explain the bounding box problem.	*CO3*	*PO1*	**10**

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