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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**

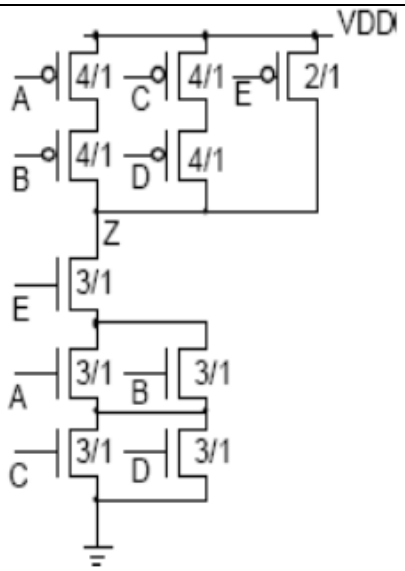
Branch: Electronics & Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 22ET7PE3AD **Max Marks: 100**

Course: ASIC Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			CO	PO	Marks
		UNIT - I			
1	a)	Draw the flow diagram for the ASIC design and explain every step. Also, comment on logical and physical design.	*CO1*	*PO1*	**10**
	b)	What are the different choices of ASIC cell libraries? Discuss each of them.	*CO1*	*PO1*	**06**
	c)	Mention the salient features of FPGA.	*CO1*	*PO1*	**04**
		OR			
2	a)	Explain gate arrays used in semi-custom ASIC design. Discuss the different types of gates in detail with relevant figures.	*CO1*	*PO1*	**12**
	b)	Discuss the advantages and disadvantages of FPGA and ASIC Design in detail. When do you design circuits using full-custom design.	*CO1*	*PO1*	**08**
		UNIT - II			
3	a)	Describe how carry save adder reduces carry rippling, in addition. Explain how 4-input CSA is constructed using 3-input CSA. What is the need for inserting latches in the 4-input CSA?	*CO2*	*PO1*	**06**
	b)	Explain Wallace Tree multiplier.	*CO2*	*PO1*	**08**
	c)	Draw a three-state bi-directional output buffer and explain how it works.	*CO2*	*PO1*	**06**
		OR			
4	a)	Derive an expression for optimum path delay using propagation delay of the logic cascade.	*CO2*	*PO2*	**08**
	b)	For a logic path with a 1X drive minimum size inverter used to drive one input of 2X drive NOR3 logic cell in C_5 technology, determine the total delay. Given logic ratio r = 1.5 and C_{out} = 0.3 pF.	*CO2*	*PO1*	**08**
	c)	For an AOI221 logic cell shown in Figure Q4(c), compute logical effort and logical area. Assume the logic ratio r = 2.	*CO2*	*PO2*	**04**

			 **Figure Q4(c)**			
			UNIT - III			
5	a)		With the help of a block diagram explain the XC3000 Logic Block. Also, discuss the different modes of operation.	*CO3*	*PO1*	**10**
	b)		Develop the timing model for ACT-2 logic modules. How do you estimate the critical path between the registers?	*CO3*	*PO1*	**10**
			OR			
6	a)		Devise the Boolean function **f = ab + b'c + d** in the ACT1 logic module.	*CO3*	*PO2*	**06**
	b)		Realize the following two-input logic gates using 2:1 MUX: i. NOR-11 ii. AND1-1 iii. OR	*CO3*	*PO2*	**06**
	c)		With of help of a suitable figure explain the logic element of Altera FLEX 80000 series FPGA.	*CO3*	*PO1*	**08**
			UNIT - IV			
7	a)		With the help of a block diagram explain Xilinx XC4000 input output block.	*CO3*	*PO1*	**12**
	b)		What is supply bounce? With the help of a suitable example explain supply bounce with relevant waveforms.	*CO3*	*PO1*	**08**
			OR			
8	a)		Explain Altera's I/O control block and I/O element with suitable block diagrams.	*CO3*	*PO1*	**12**
	b)		With suitable figure explain Xilinx LCA interconnect.	*CO3*	*PO1*	**08**

			UNIT - V			
	9	a)	What is the need for hierarchical design? Illustrate the hierarchical design for a 16-bit D latch with enable starting from primitive gates.	*CO3*	*PO2*	**12**
		b)	What is a netlist screener? Why it is used? Discuss the errors that can be found using it.	*CO3*	*PO1*	**08**
			OR			
	10	a)	What are the difficulties of using ASIC libraries? Explain with an example.	*CO3*	*PO1*	**06**
		b)	Justify the need for back-annotation in physical design flow.	*CO3*	*PO1*	**06**
		c)	Illustrate the vector instances and buses for a 16-bit D latch with enable using one bit D-latch	*CO3*	*PO2*	**08**

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