U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May / June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VIII**

Branch: Electronics and Telecommunication Engineering **Duration: 3 hrs.**

Course Code: 22ET8PE4LV **Max Marks: 100**

Course: Low Power VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Explain the classification of MOSFETs as per ITRS.	*CO1*	-	**10**
	b)		Analyze the low power IC design beyond Sub-20 nm Technology with respect to issues related to: i. Silicon Manufacturability and Variation ii. Design Productivity	*CO1*	-	**10**
			OR			
2	a)		Explain the classification of MOSFETs through deep sub-micron technology with V_{DS} vs I_{DS} graphs for each case.	*CO2*	*PO1*	**10**
	b)		Analyze the significance of following with respect to Low Power VLSI: i. Sub-threshold slope ii. Ultra-Low voltage operation	*CO1*	-	**10**
			UNIT - II			
3	a)		Analyze the importance of static logic circuit in low power VLSI.	*CO1*	-	**10**
	b)		Analyze the concept of Ratioed logic considering an inverter. Support your analysis with relevant equations.	*CO2*	*PO1*	**10**
			OR			
4	a)		Implement the following CMOS logic circuits: i. 3 input NAND gate ii. 2 input OR gate iii. $y = \overline{A + BC}$	*CO2*	*PO1*	**10**
	b)		Implement the following using Ratioed Logic: i. 3 input NOR gate ii. 2 input AND gate iii. $y = \overline{(A + B)C}$	*CO2*	*PO1*	**10**

			UNIT - III			
	5	a)	Explain the concept of signal restoring Pass transistor logic design with relevant circuit diagram.	*CO1*	-	**10**
		b)	Implement the following: i. Eight transistor CMOS TG implementation of XOR ii. TG based adder	*CO1*	-	**10**
			OR			
	6	a)	Analyze the main features of CPL and thereby implement the following using CPL technology: i. 2 input XOR/XNOR ii. Y = A+BC/$\overline{A+BC}$	*CO2*	*PO1*	**10**
		b)	Analyze the operation of a tristate buffer and tristate inverter. Implement the tristate buffer using TG.	*CO1*	-	**10**
			UNIT - IV			
	7	a)	Analyze the operation of a 2 input DTMOS NAND gate with relevant circuit diagram and timing diagrams.	*CO2*	*PO1*	**10**
		b)	Implement the following using DTMOS logic and show their timing diagrams: i. 2 input NOR gate ii. Y = $\overline{A+B(C+D)}$	*CO2*	*PO1*	**10**
			OR			
	8	a)	Implement the following using DTMOS logic and show their timing diagrams: i. 2 input NAND gate ii. 2X2 multiplier	*CO2*	*PO1*	**10**
		b)	Analyze the operation of a 4:2 Compressor Adder with its block diagram and gate level presentation.	*CO2*	*PO1*	**10**
			UNIT - V			
	9	a)	Analyze the importance of regenerative circuits. Explain the operation of a basic SR flipflop.	*CO2*	*PO1*	**10**
		b)	Analyze the operation of a clocked JK latch and implement: i. Circuit diagram using gates ii. Functional table	*CO2*	*PO1*	**10**
			OR			
	10	a)	Analyze the operation of a clocked SR latch and implement: i. Circuit diagram using gates ii. CMOS circuit iii. Timing diagram	*CO2*	*PO1*	**10**
		b)	Implement and briefly analyze the following: i. Multiplexer-based Latch ii. Positive latch built using transmission gate	*CO2*	*PO1*	**10**

****