U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES Cluster(ECE/EE/ML/ET/EI) **Duration: 3 hrs.**
Course Code: 19ES3CCAEC **Max Marks: 100**
Course: Analog Electronic Circuits **Date: 15.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Determine Vo for the network shown in figure 1. a **06**

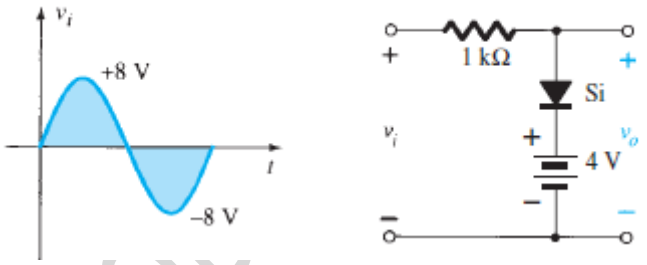


Fig 1.a

b) Derive an equation for IB and VCE of voltage divider biasing, using approximate analysis. **06**

c) Obtain the AC equivalent model of a CE voltage divider network and derive Zi, Zo, Av, AI **08**

OR

2 a) Sketch Vo for the circuit shown in figure 2.a **06**

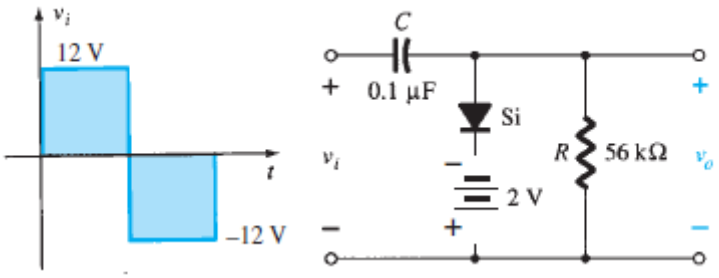


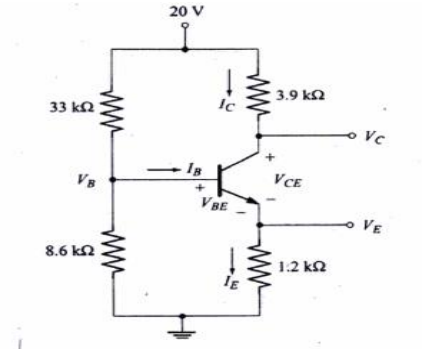
Fig 2.a

b) For the voltage divider configuration shown below , Use approximate analysis and calculate **06**

a)V_B

b)I_C and I_B

c) V_E and V_{CE}. Assume silicon transistor with β =110



c) Derive an expression for Z_i,Z_0,A_V and A_I for the voltage divider network using r_e equivalent model **08**

UNIT - II

3 a) Obtain the miller effect input and output capacitance **08**

b) Discuss the properties of negative feedback amplifier. **06**

c) Calculate the gain, input, and output impedances of a voltage-series feedback amplifier having *A* = -300, *Ri* = 1.5 kΩ, *Ro* = 50 kΩ, and β =1/15. **06**

UNIT - III

4 a) Explain the operation of a transformer coupled class B power amplifier **08**

b) Calculate the input power, output power and efficiency of the amplifier circuit shown in figure 4.b for an input voltage that results in a base current of 10mA peak. **06**

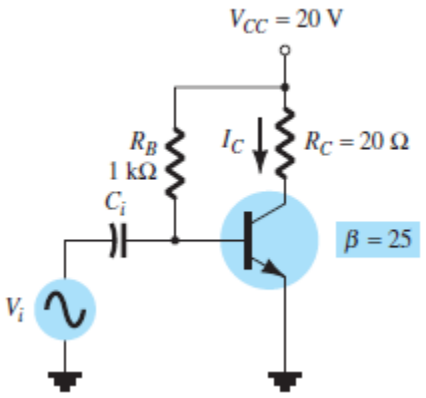


Fig 4.b

c) What is harmonic distortion? Explain the causes of distortion. **06**

UNIT - IV

5 a) Explain the following with respect to enhancement MOSFET **06**
i. Triode region

ii. Saturation region

b) Design the circuit shown in the Fig 5(b) so that the transistor operates at I_D = 0.4mA and V_D = +0.5V. The NMOS transistor has V_t = 0.7V, $\mu_n C_{ox}$ = 100μA/V², L = 1μm, and W = 32 μm. Neglect the channel length modulation effect. **06**

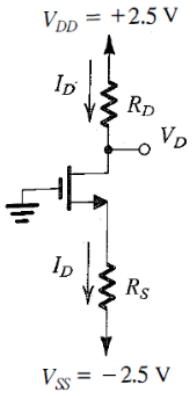


Fig 5(b)

c) Describe an arrangement to bias MOSFET using a constant current source **08**

UNIT - V

6 a) Derive an expression for g_m using small signal condition. **10**

b) Compare CS and CG amplifier **04**

c) Derive an expression for Av of a CG amplifier **06**

OR

7 a) Construct a small signal equivalent circuit of a CS amplifier with a source resistance and show its effect voltage gain **10**

b) Derive the overall gain of a source follower using small signal model of MOSFET. **10**

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