U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: ES CLUSTER (MD/EE/EI/ET) **Duration: 3 hrs.**

Course Code: 22ES3PCDCS **Max Marks: 100**

Course: Digital Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Design a logic circuit for the function using minimum number gates. F (W, X, Y, Z) = ∑ m (1, 3, 4, 11) + ∑ d (2, 7, 8, 12, 14, 15)	CO1	PO2	**08**
	b)		Simplify the following Boolean function using tabulation method. F (A, B, C, D) = ∏ M(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)	CO1	PO2	**08**
	c)		Describe different Verilog Operators.	CO1	PO2	**04**
			OR			
2	a)		Write all the prime implicants and obtain minimal sum for the Boolean function f(a,b,c,d) = ∑m(0,2,5,7,8,10,13,15)+ ∑d(1,4,11,14) using Karnaugh Map.	CO1	PO2	**05**
	b)		Use Tabulation method to find all the prime implicants for the function f(a,b,c,d) = ∑m(3,4,5,7,10,12,14,15) +∑d(2)	CO1	PO2	**07**
	c)		Discuss any 3 important data types available in Verilog. Give examples for each.	CO1	PO2	**08**
			UNIT - II			
3	a)		Design and explain the operation of 4-bit Carry look ahead adder.	CO2	PO3	**10**
	c)		Explain Data flow modeling with suitable examples.	CO2	PO3	**10**
			OR			
4	a)		Write a Verilog code that represents a full adder using dataflow description.	CO2	PO3	**08**
	b)		Explain the working of BCD adder with appropriate diagrams.	CO2	PO3	**12**

			UNIT - III			
	5	a)	Design a 3-bit gray to binary code converter and describe the behavior using data flow description.	*CO2*	*PO3*	**10**
		b)	Design the following Boolean functions using a suitable PLA. F_1 (a, b, c) = **Σ**m (0, 1, 2, 5, 7) F_2 (a, b, c) = **Σ**m (3, 4, 5) F_3 (a, b, c) = **Σ**m (3, 4, 5, 6)	*CO2*	*PO3*	**10**
			OR			
	6	a)	Design a BCD-Decimal decoder using 2 to 4 decoders.	*CO2*	*PO3*	**10**
		b)	Implement the function f(a,b,c) = ∑m(0,1,4,7)using 4:1 Mux. Take i) ab ii) bc as select lines	*CO2*	*PO3*	**10**
			UNIT - IV			
	7	a)	Obtain the characteristic equation of SR-FF.	*CO3*	*PO3*	**06**
		b)	Convert JK-FF to D-FF.	*CO3*	*PO3*	**08**
		c)	Write a Verilog code for JKFF with active low preset and clear.	*CO3*	*PO3*	**06**
			OR			
	8	a)	What is race around condition? Explain different methods to eliminate it.	*CO3*	*PO3*	**08**
		b)	Realize T-FF using D-FF.	*CO3*	*PO3*	**06**
		c)	Write a Verilog code for T-FF with active low preset and clear .	*CO3*	*PO3*	**06**
			UNIT - V			
	9	a)	Write a Verilog code for 4-bit Johnson counter.	*CO3*	*PO3*	**04**
		b)	Design a synchronous counter using T-FFs for the sequence 0, 1, 2, 4, 6, 0, 1,……	*CO3*	*PO3*	**08**
		c)	With a neat diagram explain the operation of 4-bit universal shift register.	*CO3*	*PO3*	**08**
			OR			
	10	a)	Write a Verilog code for BCD up-downcounter.	*CO3*	*PO3*	**08**
		b)	Design 2-bit up-down counter using D-FFs.	*CO3*	*PO3*	**06**
		c)	Design a MOD- 10 Ripple counter.	*CO3*	*PO3*	**06**

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