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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES CLUSTER (EEE/ ETE /MD /EIE) **Duration: 3 hrs.**
Course Code: 22ES3PCDCS **Max Marks: 100**
Course: Digital Circuits **Date: 12.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Simplify the function f (A, B, C, D) = ABC + AB +A'BC'D' + BC' using Karnaugh map. Design a circuit for the same using only NAND gates. **08**

b) NASA consists of four computers out of which two are connected to the space craft at any given time and remaining two computers are used to ensure safety operation in case if any one fails. Design a low cost logic circuit which sends a warning signal if two or more computers fail. ("HIGH" signal indicate a working computer, while "LOW" signal indicate a failing computer). **07**

c) With X= 4'b1101, Y=3'b110, Z=3'b010 obtain **05**
i) {X,Y,Z}
ii) X^Y
iii) ~(X&Y)
iv) Z<<3
v) &(X)

UNIT - II

2 a) Design a single digit BCD adder to add given two decimal numbers. **07**

b) Develop Verilog code for a full subtractor using dataflow style. **06**

c) Design 3-bit carry lookahead adder and prove that propagation delay is constant irrespective of number of stages. **07**

UNIT - III

3 a) Design 16:1 multiplexer using 4:1 multiplexer. Write its truth table and demonstrate its working for any one input combination. **07**

b) Realize the following using PLA: **07**
$F0(a,b,c) = \sum m(0,\ 2,4,6)$
$F1(a,b,c) = \sum m(2,4,5,6,7)$
$F2(a,b,c) = \sum m(\ 0,1,2,4)$

c) Design a 2 to 4 decoder using Verilog dataflow modeling. Consider an enable input to activate the decoder. **06**

UNIT - IV

4	a)	Derive the characteristic equations of D, JK, T and SR flip flops.	**08**
	b)	Realize (i) JK flip flop from D flip flop (ii) T flip flop from D flip flop (iii) D flip flop from JK flip flop.	**06**
	c)	Develop the Verilog code for D flip flop using behavioral style.	**06**

OR

5	a)	Design master slave JK flip flop. Write its function table and explain its working with waveforms.	**07**
	b)	Design gated SR latch and gated D latch. Write its function table and discuss the limitations of gated latch.	**07**
	c)	Develop the Verilog code for JK flip flop using case statement.	**06**

UNIT - V

6	a)	Design a 3-bit universal shift register using D flip flops and Multiplexers (with S1 and S0 as select lines) to perform the following functions:	**07**

Sl. no	S1	S0	Register operation
1	0	0	Hold
2	0	1	Shift right
3	1	0	Shift left
4	1	1	Parallel load

	b)	Construct a 4-bit binary ripple counter using positive edge triggered T flip flop. Write its truth table and demonstrate its working with timing diagrams.	**07**
	c)	Develop a Verilog code for 4-bit up/down counter. Use the control bit 'Dir', if Dir=0 implies up counting while Dir=1 implies down counting.	**06**

OR

7	a)	Design a 4-bit synchronous down counter using T flip-flop.	**08**
	b)	Design 4-bit shift register (i) SIPO (ii) SISO (iii) PIPO.	**06**
	c)	Develop a Verilog code for 4:1 mux using structural style.	**06**

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