U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: ES CLUSTER (EEE/ ETE /MD/EIE) **Duration: 3 hrs.**
Course Code: 22ES3PCDCS **Max Marks: 100**
Course: Digital Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Find the minimized expression for the following function using tabular method f(w,x,y,z)= ΠM (0,4,7,5,9) . Π d (1, 7, 13).	**10**
	b)	Simplify the following expression using K-map. F(A,B,C,D)=Σm(1,2,4,11,13,14,15)+ Σd(0,5,7,8,10).	**06**
	c)	Obtain the syntax for a Verilog module.	**04**

UNIT - II

2	a)	Design a 4-bit carry look adder and mention its advantages over conventional adder circuits.	**10**
	b)	Model a Verilog code for all the basic gates in different modules using data flow description.(any 5)	**10**

UNIT - III

3	a)	Implement f(a,b,c,d)= Σm(0,1,5,6,7,10,15) using 4:1 Multiplexer.	**05**
	b)	Implement the following function f1(x,y,z)= Σm(1,2,3,7) and f2= Σm(0,1,2,6) using 3x4x2 PLA.Write the PLA table.	**08**
	c)	Design and write VERILOG code to implement the functionality of a 1-Bit comparator using data flow description.	**07**

UNIT - IV

4	a)	Explain the working of a positive edge triggered D-flip-flop.	**06**
	b)	Write the characteristic equations and excitation tables for the following flip-flops. i) J-K Flip-flop ii) D Flip-flop	**07**
	c)	Design and write Verilog code to implement the functionality for a JK Flip Flop.	**07**

OR

5	a)	Explain the working of JK Flip-flop using NAND gates with its truthtable.What is the problem associated with the circuit. Explain how it can be avoided.	**08**

b) Conclude on the time period of the clock (clk) generated by the following code segment? **05**

```
initial
#2 clk = 1'b0;
always
#10 clk = ~clk;
```

c) Convert JK flip-flop to AB flip-flop. Functional table of AB flip-flop is described in the table below. **07**

A	B	Q^+
0	0	0
0	1	Q'
1	0	Q
1	1	1

UNIT - V

6 a) Design and write VERILOG code to implement the functionality of a 4-bit Ripple Carry Adder using and Structural Architecture. **10**

b) Design a 3-bit synchronous up-counter using D Flip-flop. **10**

OR

7 a) Design and write Verilog code for 16-to-1 Multiplexer using structural modeling using behavioral modeling of 4-to-1 Multiplexer. **10**

b) Design a Universal shift Register for the following condition: **10**
The CLRb input is asynchronous and active low and overrides all the other inputs. All other states changes following the rising edge of the clock. If the control inputs S1=S0=1, the register is load in parallel. If S1=1 and S0=0, the register is shifted right and SDR (Serial data right) is shifted into Q3. If S1=0 and S0=1, the register is shifted left and SDL is shifted into Q0. If S1=S0=0, no action occurs.

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