U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES CLUSTER (EEE/ETE/MD/EIE) **Duration: 3 hrs.**
Course Code: 22ES3PCDCS **Max Marks: 100**
Course: Digital Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Obtain minimal sum and minimal product for the Boolean function $f(a,b,c,d) = \sum m(2,4,5,6,10) + \sum d(12,13,14,15)$ using Karnaugh Map.	**08**
	b)	Use Tabulation method to find a minimal sum for the function $f(a,b,c,d) = \sum m(0,2,4,5,7,8,9,15)$	**08**
	c)	What are the different data types available in Verilog?	**04**

UNIT - II

2	a)	Explain the working of BCD adder with appropriate diagrams.	**12**
	b)	Write a Verilog code that represents a full subtractor using dataflow description.	**08**

UNIT - III

3	a)	Implement the function $f(a,b,c) = \sum m(0,1,2,7)$ using 4:1 Mux. Take i) ab ii) bc as select lines	**06**
	b)	Implement the functions f1 and f2 using a 3x4x2 PLA with true/complemented outputs. Also write the PLA table. Given: $f1(a,b,c) = \sum m(0,1,3,5)$ $f2(a,b,c) = \sum m(0,2,3,4)$	**08**
	c)	Write a Verilog dataflow code to implement an n-bit Binary to Gray code converter.	**06**

UNIT - IV

4	a)	Derive the characteristic equation of i) SR Flip flop ii) JK Flip flop	**06**
	b)	Explain the working of JK Master Slave Flip flop with neat logic diagram and timing diagrams.	**08**
	c)	Write a Verilog code to implement the functionality of D Flipflop having an active low reset (rst) and active low preset (pr). Assume the flip flop to be positive edge triggered.	**06**

OR

5	a)	Design a positive edge triggered JK Flip flop using a positive edge triggered D Flip flop.	**05**
	b)	Explain the working of a positive edge triggered D Flip flop with an appropriate logic diagrams.	**08**
	c)	Write a behavioural Verilog code to implement the functionality of a JK Flip flop	**07**

UNIT - V

6	a)	Design a Mod 10 asynchronous counter using positive edge triggered T flip-flops. Draw the timing diagrams and also write the counting sequence.	**07**
	b)	With relevant logic diagrams and examples explain different modes of operation of 4-bit Unidirectional shift register for both parallel and serial data transfer.	**08**
	c)	Write a gate-level Verilog code for a full adder.	**05**

OR

7	a)	Design a synchronous Mod 5 counter for the following counting sequence 0,2,3,5,7,0, 2…. and repeat. Use D flip flops having outputs $Q_A Q_B Q_C$.	**08**
	b)	Draw the logic diagram of a 3-bit shift register using D Flip-flops. Show how it can be used as a ring counter and as a twisted ring counter. Write the counting sequence and indicate their mod numbers.	**07**
	c)	Write a gate-level Verilog code for a 2x1 Mux.	**05**

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