U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2023 Semester End Make-Up Examinations

Programme: B.E.
Branch: ES CLUSTER (EEE/ ETE /MD/EIE)
Course Code: 22ES3PCDCS
Course: Digital Circuits

Semester: III
Duration: 3 hrs.
Max Marks: 100
Date: 10.08.2023

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Design a logic circuit for the function F (W, X, Y, Z) = $\prod M$((1, 3, 4, 11). $\prod d$ (2, 7, 8, 12, 14, 15) using minimum number gates		08
	b)	Simplify the following Boolean function using tabulation method. F (A, B, C, D) = $\sum$ m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)		08
	c)	Describe different Verilog Operators		04

UNIT - II

2	a)	Design and explain the operation of 1-digit BCD adder		10
	b)	Design a full subtractor and hence describe the behavior using data flow description		06
	c)	Explain Data flow modeling		04

UNIT - III

3	a)	Design a 3-bit binary to gray code converter and hence describe the behavior using data flow description		08
	b)	Design the following Boolean functions using a suitable PLA. F_1 (a, b, c) = Σm (0, 1, 2, 5, 7) F_2 (a, b, c) = Σm (3, 4, 5) F_3 (a, b, c) = Σm (3, 4, 5, 6)		06
	c)	Design a BCD-Decimal decoder using 2 to 4 decoders		06

UNIT - IV

4	a)	Explain the working of a positive edge triggered D-flip flop.		06
	b)	Convert JK-FF to SR-FF		06
	c)	Write a Verilog code for JKFF with active low preset and clear		08

OR

5	a)	What is race around condition? Explain different methods to eliminate it.		08
	b)	Realize T-FF using D-FF		06

	c)	Write a Verilog code for T-FF	**06**

UNIT - V

6	a)	Write a Verilog code for 4-bit Ring counter	**05**
	b)	Design a synchronous counter using D-FFs for the sequence 0, 1, 2, 4, 6, 0, 1,.....	**08**
	c)	With a neat diagram explain the operation of 4-bit universal shift register	**07**

OR

7	a)	Write a Verilog code for 4-bit Johnson counter.	**06**
	b)	Design 2-bit up-down counter using T-FFs	**08**
	c)	Design a MOD- 10 Ripple counter	**06**

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