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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## June 2025 Semester End Main Examinations

**Programme: B.E.** **Semester: V**

**Branch: ES CLUSTER (MD/EE/EI/ET)** **Duration: 3 hrs.**

**Course Code: 22ES3PCDCS** **Max Marks: 100**

**Course: Digital Circuits**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.





| | | | **UNIT - I** | *CO* | *PO* | **Marks** |
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| 1 | a) | Write all the prime implicants and obtain minimal sum for the Boolean function f(a,b,c,d) = ∑m(0,2,5,7,8,10,13,15)+ ∑d(1,4,11,14) using Karnaugh Map. | *CO1* | *PO2* | **05** |
| | b) | Use Tabulation method to find all the prime implicants for the function f(a,b,c,d) = ∑m(3,4,5,7,10,12,14,15) +∑d(2) | *CO1* | *PO2* | **07** |
| | c) | Discuss any 3 important data types available in Verilog. Give examples for each. | *CO1* | *PO2* | **08** |
| | | **OR** | | | |
| 2 | a) | A 4-bit binary number is represented as $A_3A_2A_1A_0$, where $A_3$ is MSB and $A_0$ is LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than or equal to 6 and less than or equal to 12. Obtain the output expression using K-map. | *CO1* | *PO2* | **10** |
| | b) | Simplify the given expression using K-map to get the minimal sum expression and build the digital system using logical gates. f(w,x,y,z)=∑m( 3,4,6,9,11,12,13,14,15) | *CO1* | *PO2* | **10** |
| | | **UNIT - II** | | | |
| 3 | a) | Write a Verilog code that represents a full adder using dataflow description. | *CO2* | *PO3* | **08** |
| | b) | Explain the working of BCD adder with appropriate diagrams. | *CO2* | *PO3* | **12** |
| | | **OR** | | | |
| 4 | a) | Design 3-bit carry look ahead adder with expressions. | *CO2* | *PO3* | **10** |
| | b) | Develop Verilog code for the logic circuit shown in Figure 2c using dataflow modeling. | *CO2* | *PO3* | **10** |

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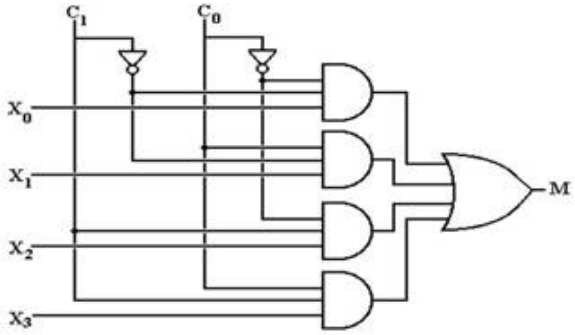
| | | |  Figure 2c | | | |
| | | | **UNIT - III** | | | |
| | 5 | a) | Implement the function f(a,b,c) = ∑m(0,1,4,7)using 4:1 Mux. Take i) ab ii) bc as select lines | *CO2* | *PO3* | **06** |
| | | b) | Implement the functions f1 and f2 using a 3x4x2 PLA with true/complemented outputs. Also write the PLA table. Given: f1(a,b,c) = ∑m(0,1,3,5) f2(a,b,c) = ∑m(3,5,7) | *CO2* | *PO3* | **08** |
| | | c) | Construct a 4 to 16 line decoder by appropriately configuring 3 to 8 line decoders. | *CO2* | *PO3* | **06** |
| | | | **OR** | | | |
| | 6 | a) | Construct a 16-to-1 line multiplexer using the 4-to-1 line multiplexers. | *CO2* | *PO3* | **10** |
| | | b) | Design a 3-bit gray to binary code converter and describe the behavior using data flow description. | *CO2* | *PO3* | **10** |
| | | | **UNIT - IV** | | | |
| | 7 | a) | Derive the characteristic equation of i)T Flip flop ii)JK Flip flop | *CO3* | *PO3* | **06** |
| | | b) | Explain the working of JK Master Slave Flip flop with neat logic diagram and timing diagrams. | *CO3* | *PO3* | **08** |
| | | c) | Write a Verilog code to implement the functionality of a binary to Gray code converter. | *CO3* | *PO3* | **06** |
| | | | **OR** | | | |
| | 8 | a) | Design a positive edge triggered JK Flip flop using a positive edge triggered SR Flip flop. | *CO3* | *PO3* | **05** |
| | | b) | Explain the working of a positive edge triggered D Flip flop with an appropriate logic diagrams. | *CO3* | *PO3* | **08** |
| | | c) | Write a behavioural Verilog code to implement the functionality of a 4 bit synchronous counter. | *CO3* | *PO3* | **07** |
| | | | **UNIT - V** | | | |
| | 9 | a) | Design a Mod 8 asynchronous up counter using positive edge triggered T flip-flops. Draw the timing diagrams and also write the counting sequence. | *CO3* | *PO3* | **05** |

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| | | b) | With relevant logic diagrams and examples explain different modes of operation of 4-bit Unidirectional shift register for both parallel and serial data transfer. | *CO3* | *PO3* | **10** |
| | | c) | Write a structural Verilog code for a a 4:1 Mux. | *CO3* | *PO3* | **05** |
| | | | **OR** | | | |
| | 10 | a) | Design a synchronous Mod 5 counter for the following counting sequence 0,3,7,6,5,0…. and repeat. Use D flip flops having outputs $Q_3Q_2Q_1$. | *CO3* | *PO3* | **08** |
| | | b) | Draw the logic diagram of a 3 bit shift register using D Flip-flops. Show how it can be used as a ring counter and as a twisted ring counter. Write the counting sequence for both. | *CO3* | *PO3* | **08** |
| | | c) | Write a structural Verilog code for a full adder. | *CO3* | *PO3* | **04** |

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