U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: (ES Cluster EE/MD/ET/EI/EC) **Duration: 3 hrs.**
Course Code: 19ES3CCDEC **Max Marks: 100**
Course: Digital Electronic Circuits **Date: 30.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Find the minimized expression for the following function using tabular method $F(W,X,Y,Z)=\Sigma m(0,3,5,6,7,10,12,13)+ \Sigma d(2,9,15)$.	**10**
	b)	Simplify the following expression using K-map. $F(W,X,Y,Z)=\Pi M(0,3,4,7,8,10,12,14))+ \Pi d(2,6)$.	**05**
	c)	Three input variables A, B and C are available. The output is equal to '1' if the input variables have more 1's than 0's. The output is '0' otherwise. Derive the expression and write the circuit for the same.	**05**

UNIT - II

2	a)	Design a combinational circuit to produce the 2's complement of a 4-bit-binary number.	**10**
	b)	Implement the following functions using appropriate PLA. $f1(x,y,z)= \Sigma m(3,6,7)$ $f2(x,y,z)= \Sigma m(0,1,2,6,7)$ $f3(x,y,z)= \Sigma m(0,1,3,4,5)$ Draw the logic diagram of the realization in PLD notation.	**10**

OR

3	a)	Implement a full adder using two 4:1 Multiplexer.	**07**
	b)	Construct a 3-to-8 line decoder with the use of a 2-to-4 line decoder.	**06**
	c)	Design a comparator to check if two n-bit numbers are equal. Configure this using cascaded stages of 1-bit comparators.	**07**

UNIT - III

4	a)	Explain the working of a positive edge triggered D-flip-flop.	**06**

b) Write the characteristic equations and excitation tables for the following flip-flops. **06**

i) J-K Flip-flop ii) D Flip-flop

c) Explain the working of JK Flip-flop using NAND gates with its truth table. What is the problem associated with the circuit. Explain how it can be avoided. **08**

OR

5 a) Design a Mod-6 asynchronous down counter using positive edge triggered J-K Flip-flops with the initial state as 111. Draw the timing diagram for the same. **05**

b) Draw a 3 bit right shift register using D Flip-flops. Show how it can be used as a twisted ring counter. **04**

c) Design a synchronous Mod-8 down counter using J-K Flip-flop. **11**

UNIT - IV

6 a) Realize the system represented by the following state diagram shown in Fig. 6a using T Flip-flops. **12**

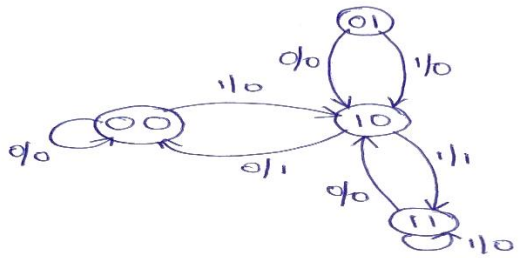

Fig. 6a.

b) With diagrams, explain the different types of sequential machines. **08**

UNIT - V

7 a) Define the following parameters **10**

i)Propagation delay

ii)Power dissipation

iii)Speed-power product

iv)Fan-out

v)Noise Margin

b) With neat logic circuit explain **10**

i) Two input CMOS NOR gate.

ii) Two input TTL NAND gate.

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