U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES CLUSTER(ECE/EE/ML/ET/EI) **Duration: 3 hrs.**
Course Code: 19ES3CCDEC **Max Marks: 100**
Course: Digital Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Solve the given expressions with Boolean simplification: **06**
i) $x\ (\bar{x}+ y)$
ii) $C + \overline{(BC)}$
iii) $\overline{AB}(\bar{A} + B)(\bar{B} + B)$

b) Simplify the Boolean function using K-map and write the circuit diagram for the same. **06**
$F\ (w, x, y, z) = \sum m(1, 3, 7, 11, 15) + \sum d(0,2,5)$

c) Simplify the Boolean function $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + \sum d(2,4)$ using Tabular method. **08**

UNIT - II

2 a) Explain 4 bit Carry look ahead adder with suitable equations and logic diagram. **10**

b) Implement the following function $F(A,B,C,D)=\sum m(0,1,2,4,6,9,12,14)$ using 4:1 mux considering A & B as select lines. **10**

OR

3 a) Describe the 4 bit ripple carry adder. **10**

b) Implement the following function using a PROM **10**
F1 (A,B,C) = AB + B'C
F2 (A,B,C) = $(A + B' + C)(A'$+B)
F3 (A,B,C) = A+BC

UNIT - III

4 a) With a neat circuit diagram, explain the functioning of SR latch with enable input. **10**

b) Derive the characteristic equation and excitation table for D flip flop & T flip-flop. **10**

OR

5	a)	Draw the timing diagram and explain the master slave JK flip-flop	**10**
	b)	Describe how SR latch can be used as switch debounce circuit.	**10**

UNIT - IV

6	a)	Analyze and Design MOD-8 Up-Counter using JK flip flop and draw the timing diagram for the same.	**10**
	b)	Design a non-overlapping Mealy sequence detector for the sequence 101 using JK flip flops.	**10**

UNIT - V

7	a)	Discuss 2 input NAND and NOR CMOS logic with neat circuit diagram.	**10**
	b)	Write a short note on: 1. Fan in 2. Fan out 3. Propogation delay 4. Power dissipation 5. Noise margin	**10**

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